Instruction Packing for a 32-bit Resource Efficiency Processor

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Topics

- SMC Processor Design
- VY Processor Design
- Experiment: SMC vs VY
- Result
  - Performance
  - Program’s size

SMC Processor

- Stack-based architecture
- 16-bit processor
- von Neumann architecture
- No pipeline, no interrupt

SMC Instruction Set

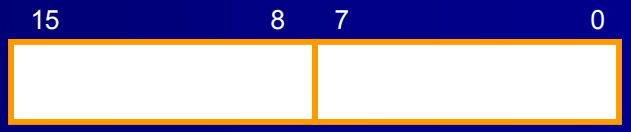
- Stack-based instruction set called “Bytecode”
- 25 instructions separate into 3 sets
  - Arithmetic and Logic
  - Data Transfer
  - Control flow

SMC Bytecode Format

- Three formats

No operand

One-byte operand



Two-byte operand

VY Processor

- Design based on SMC
- 32-bit stack-based processor
- Modified from SMC
  - Data path
  - Change bytecode format to support 32-bit processing
  - Adding some necessary bytecode into instruction set
  - Instruction packing

VY Bytecode

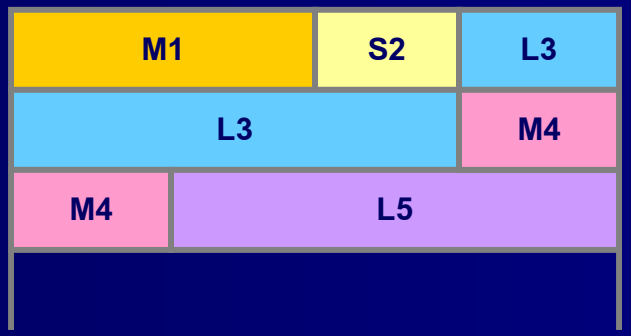
- There are three formats like the SMC

- 40 Instructions

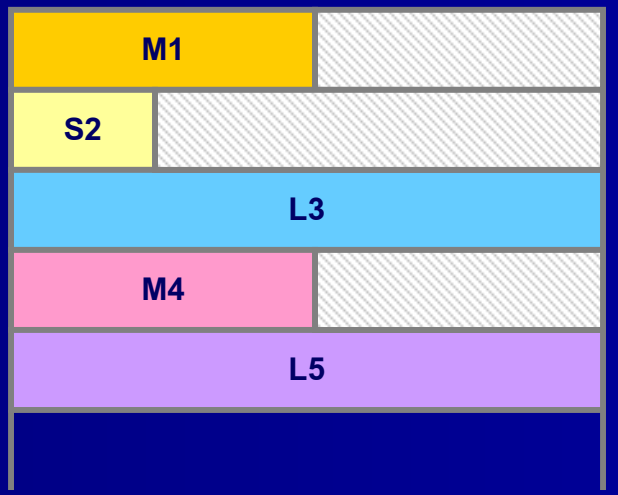
Modification from SMC

- Modified the data path
  - Put the PC out of Register file
  - 2-phase clock
- Adding more bytecode for decrease the program's size and increase the performance
- Instruction packing

Instruction Packing

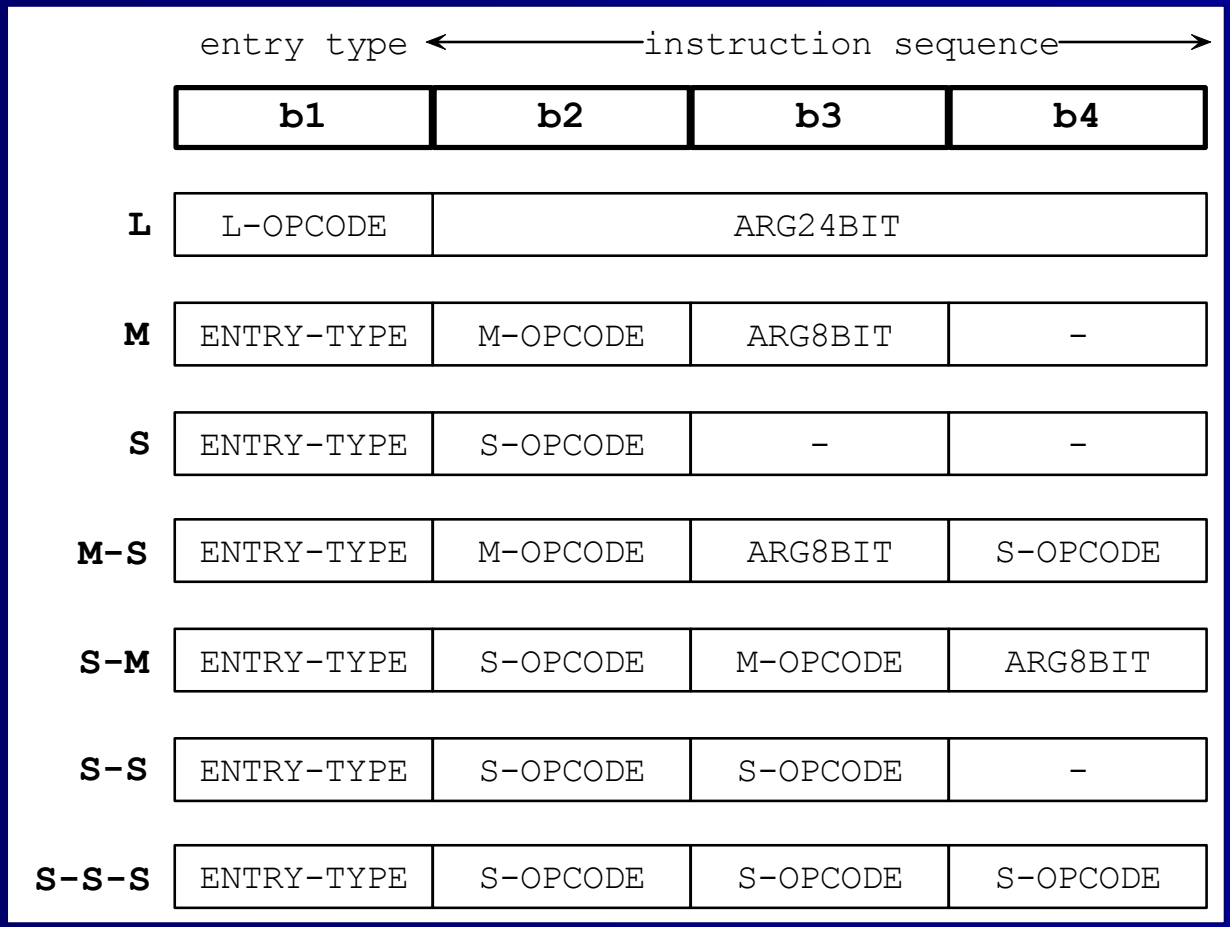


- Variable length
- Save the memory
- Slow fetching

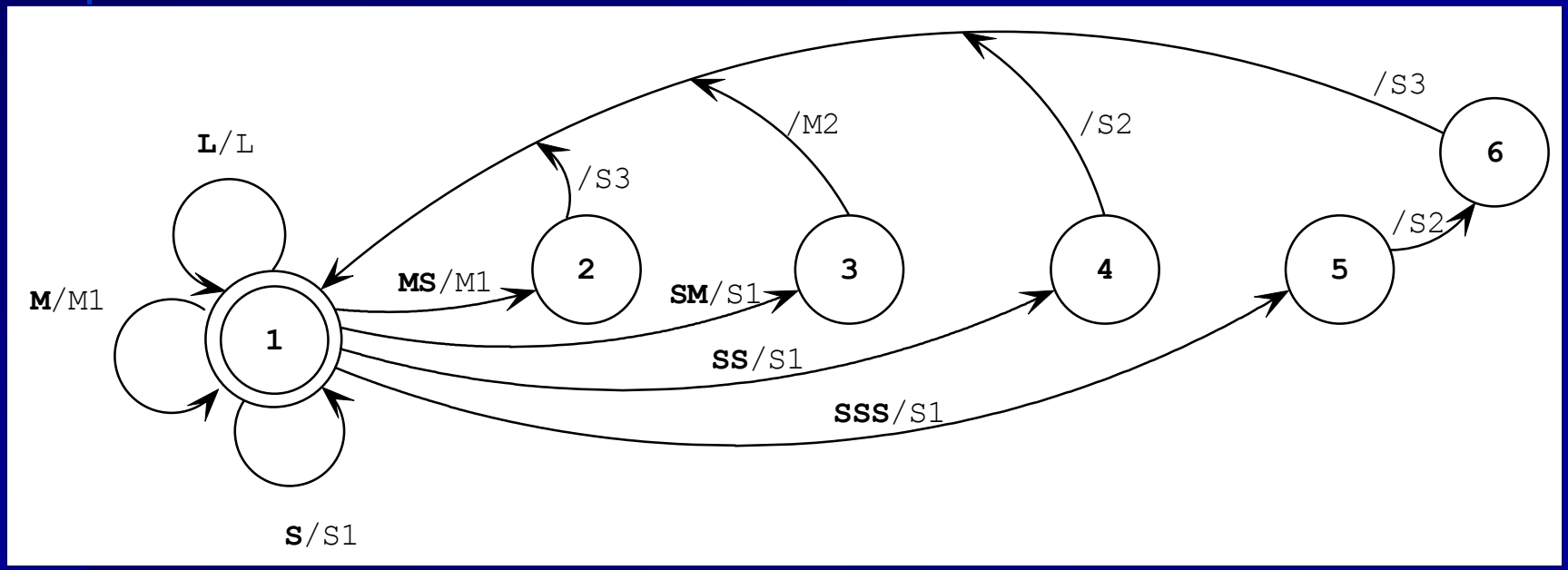


- 32-bit fix length
- One clock fetch
- Large memory size

Instruction Packing Format



Decoding and Execution

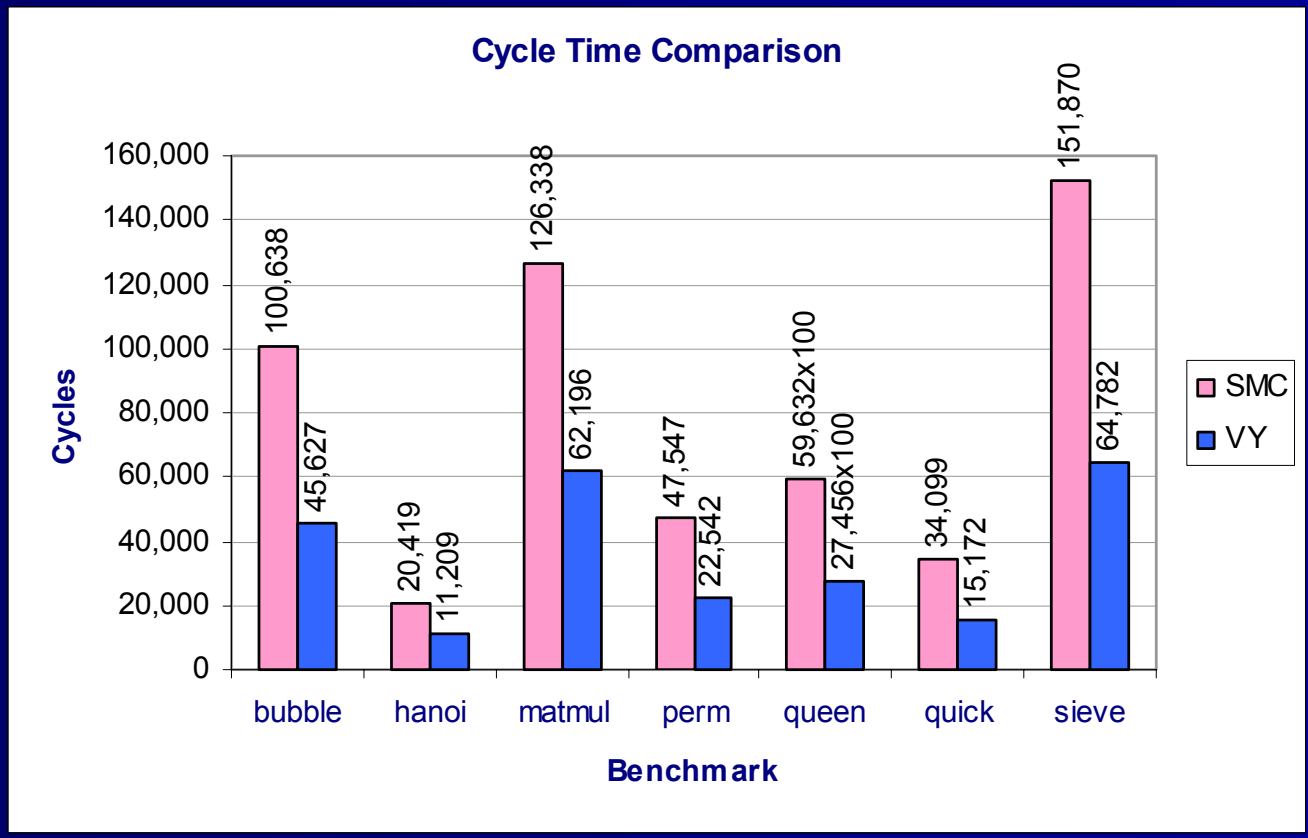


Experiment

- Simulate the SMC and VY processor
- Stanford's integer benchmark
  - Compiled into each processor
- Compare between VY and SMC (2-phase):
  - Performance
  - Program's size

Result: Performance

- Ratio of cycle time between VY and SMC is 2.12
- CPI of VY is 4.99, SMC is 8.61

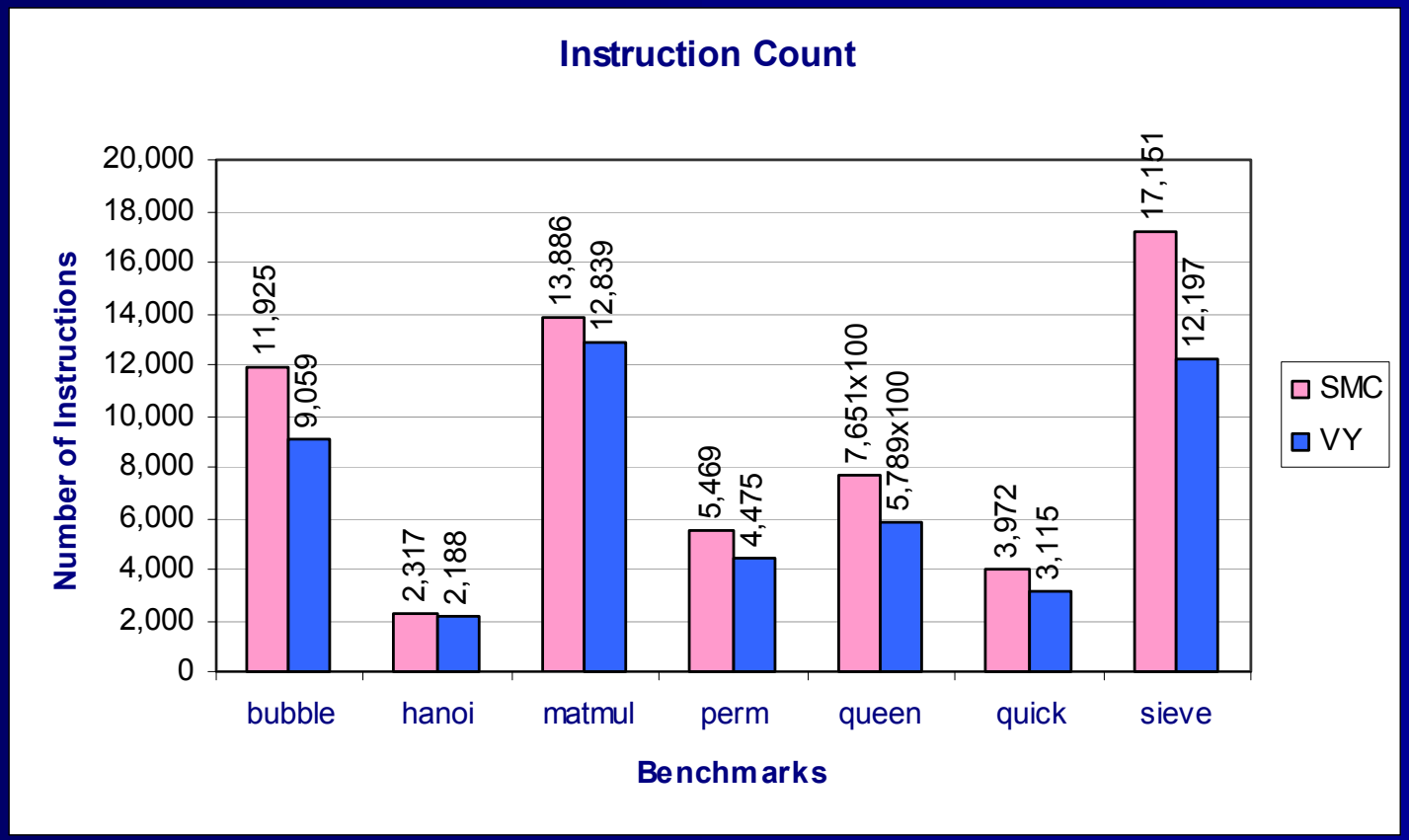


Result: Time for Fetching

Benchmark	SMC %Fetch	VY %Fetch
bubble	55	32
hanoi	54	31
matmul	56	32
perm	56	33
queen	55	34
quick	56	33
sieve	55	32
Average	**55**	**32**

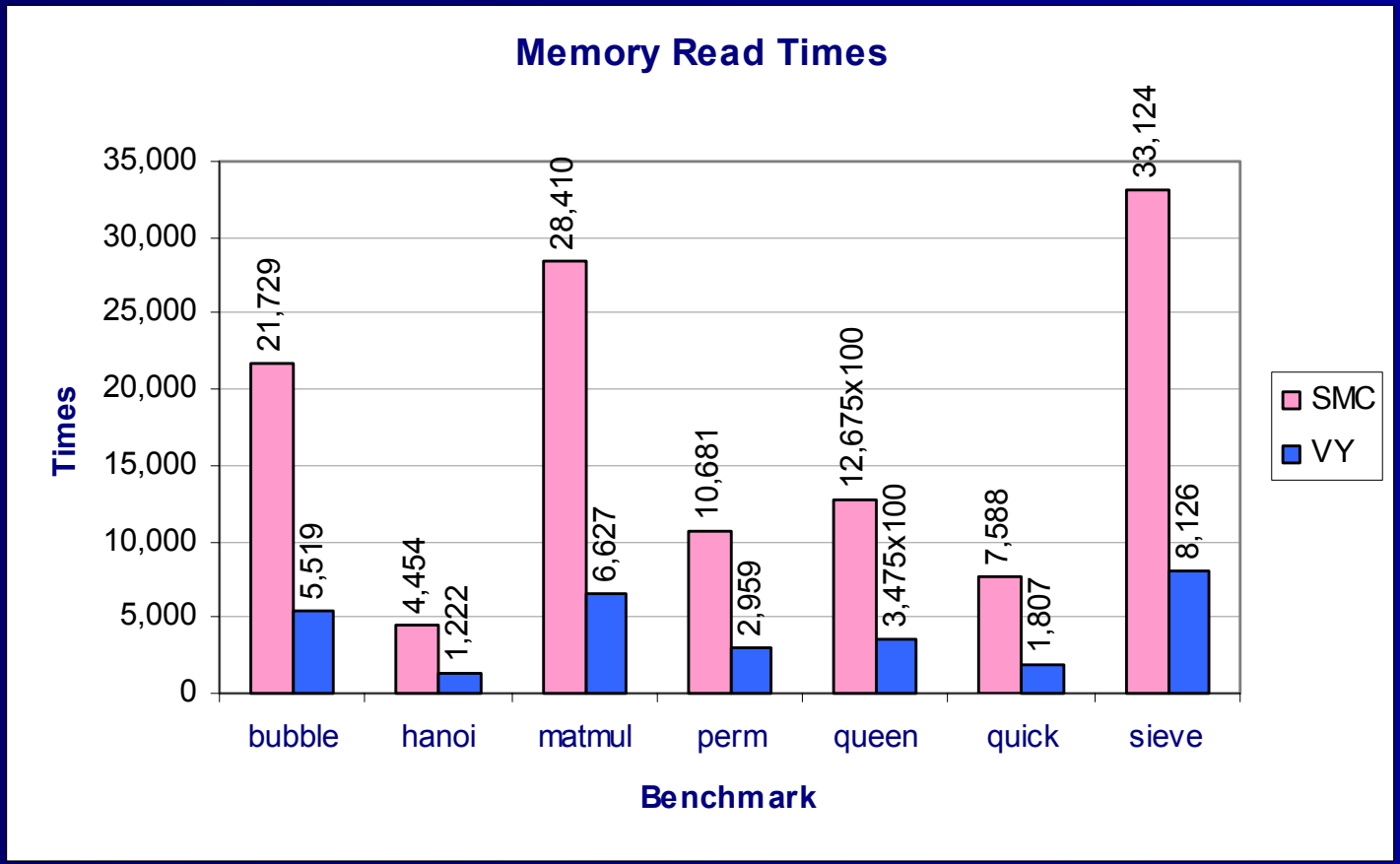
Result: Instruction Count

- VY is 81% of SMC

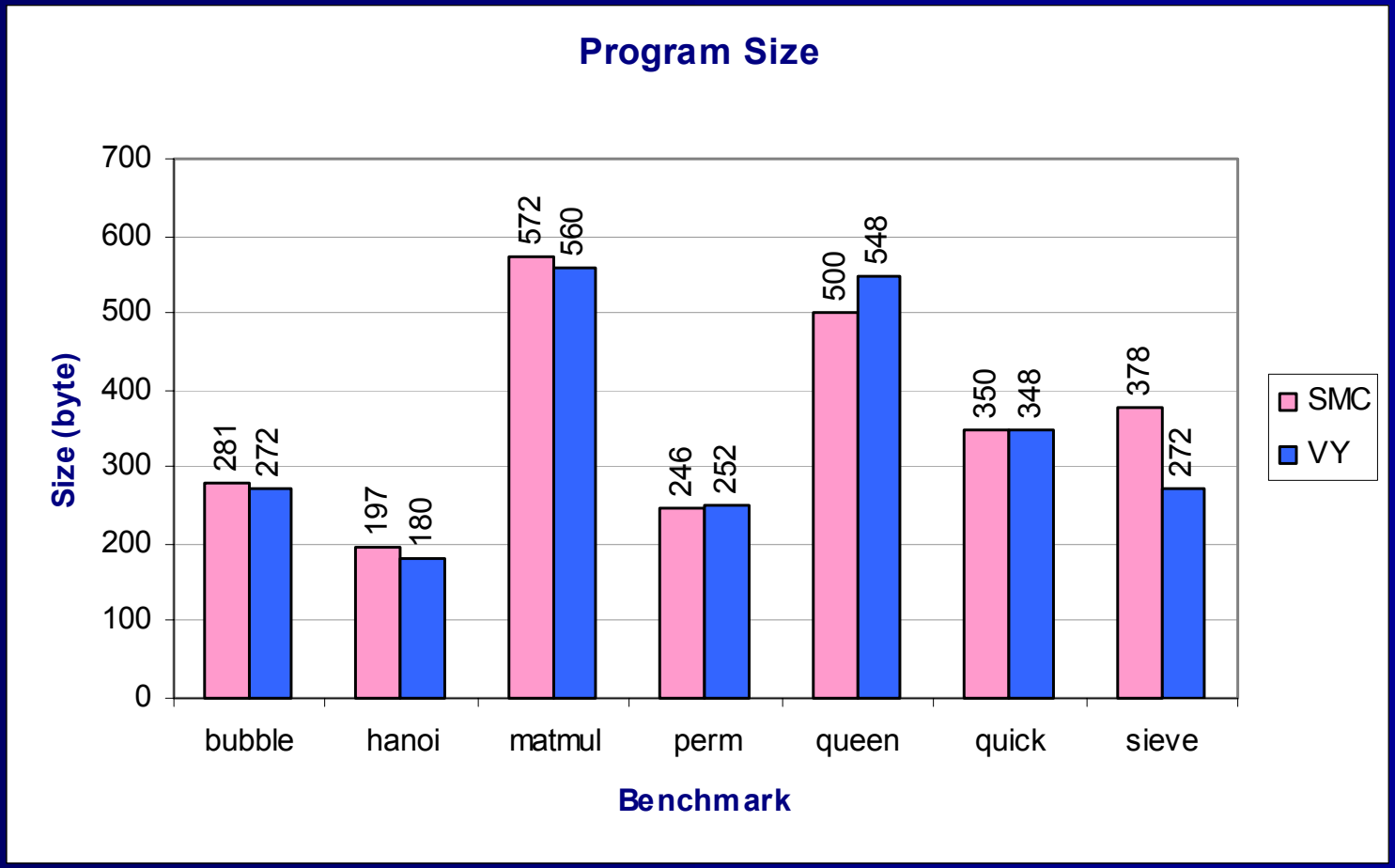


Result: Memory Read

- VY is 25% of SMC



Result: Program Size



Result: NOP Byte Space

Benchmarks	VY (byte)	NOP (Byte)	%NOP
bubble	272	34	12.5%
hanoi	180	15	8.33%
matmul	560	61	10.89%
perm	252	32	12.70%
queen	548	75	13.69%
quick	348	40	11.49%
sieve	272	36	13.24%
NOP Byte Average			**11.83%**

Conclusion

- Design of 32-bit stack processor
- Instruction packing, modification of data path and bytecode adding plays an important role in
  - Increasing the performance 2.12 times of SMC
  - Keeping the small program's size

Future Work

- Develop this design to run in FPGA
- Apply the stack caching model into this design

Question?