A Low-Power Single-Ended Virtually-Grounded-Drain Class AB Switched-Current Memory Cell with Low Charge- Injection, Clock-Feedthrough and Conduction Errors

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1.1 Reviews on 3G Mobile Systems : Evolution of 3G Mobile Systems

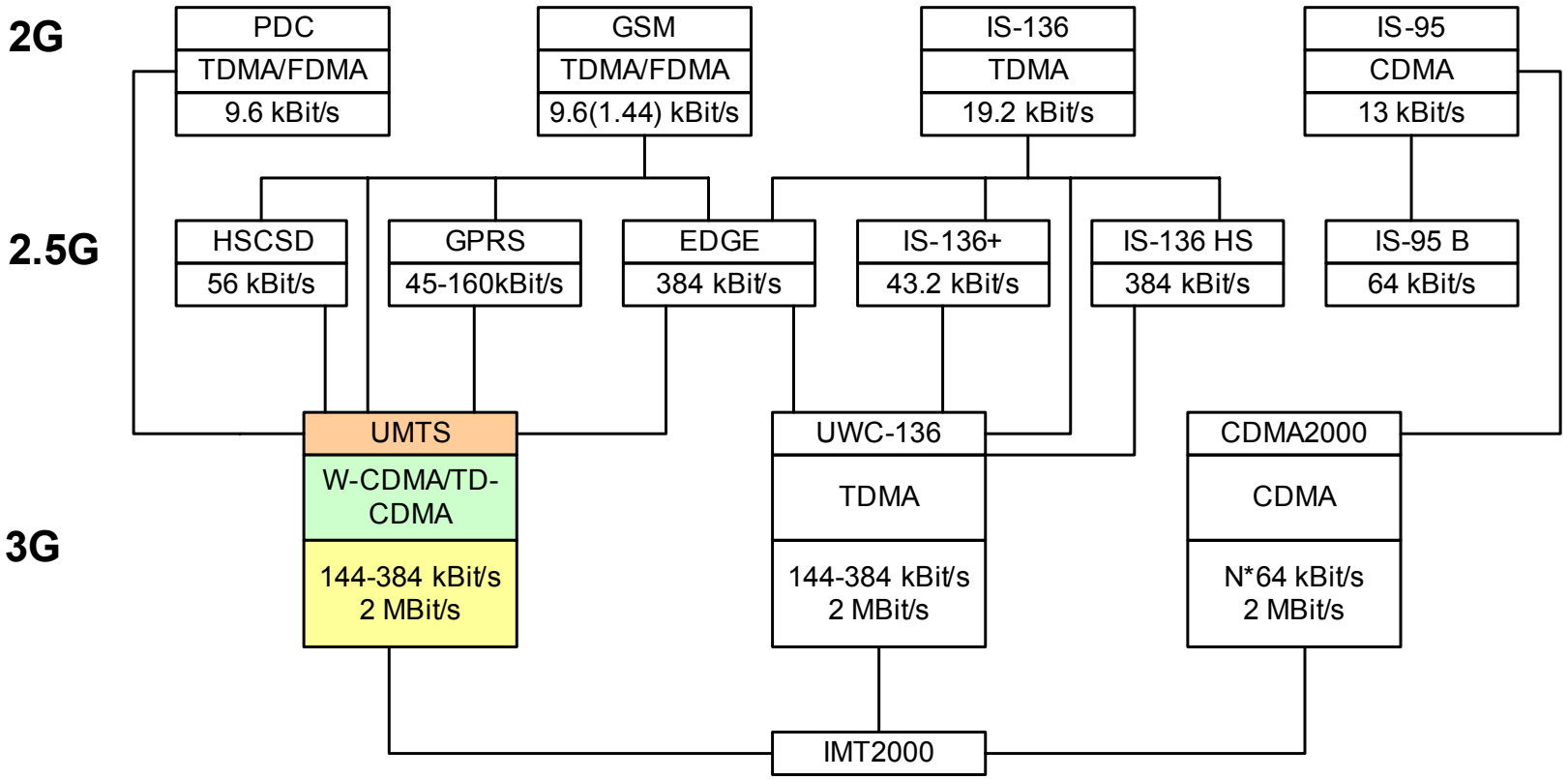


Fig. 1. Evolution toward third-generation mobile systems.

Ref: Wolfgang et al. , IEEE Journal of solid-state Circuits,Vol.36, No. 9, September 2001

1.Introductions

1.1 Reviews on 3G Mobile Systems : Parameters and Requirements

Table. 1. Parameters and system requirements for W-CDMA.

Parameters	W-CDMA Requirements
Uplink	1,920 – 1,980 MHz
Downlink	2,110 – 2,170 MHz
Modulation	QPSK
Channel data clock rate	3.84 Mchip/s
Bandwidth	5 MHz
Access Method	DS-CDMA
Duplex	FDD

Ref: Wolfgang et al. , IEEE Journal of solid-state Circuits,Vol.36, No. 9, September 2001

1.Introductions

1.2 Front - End Receiver Architectures: Direct Conversion

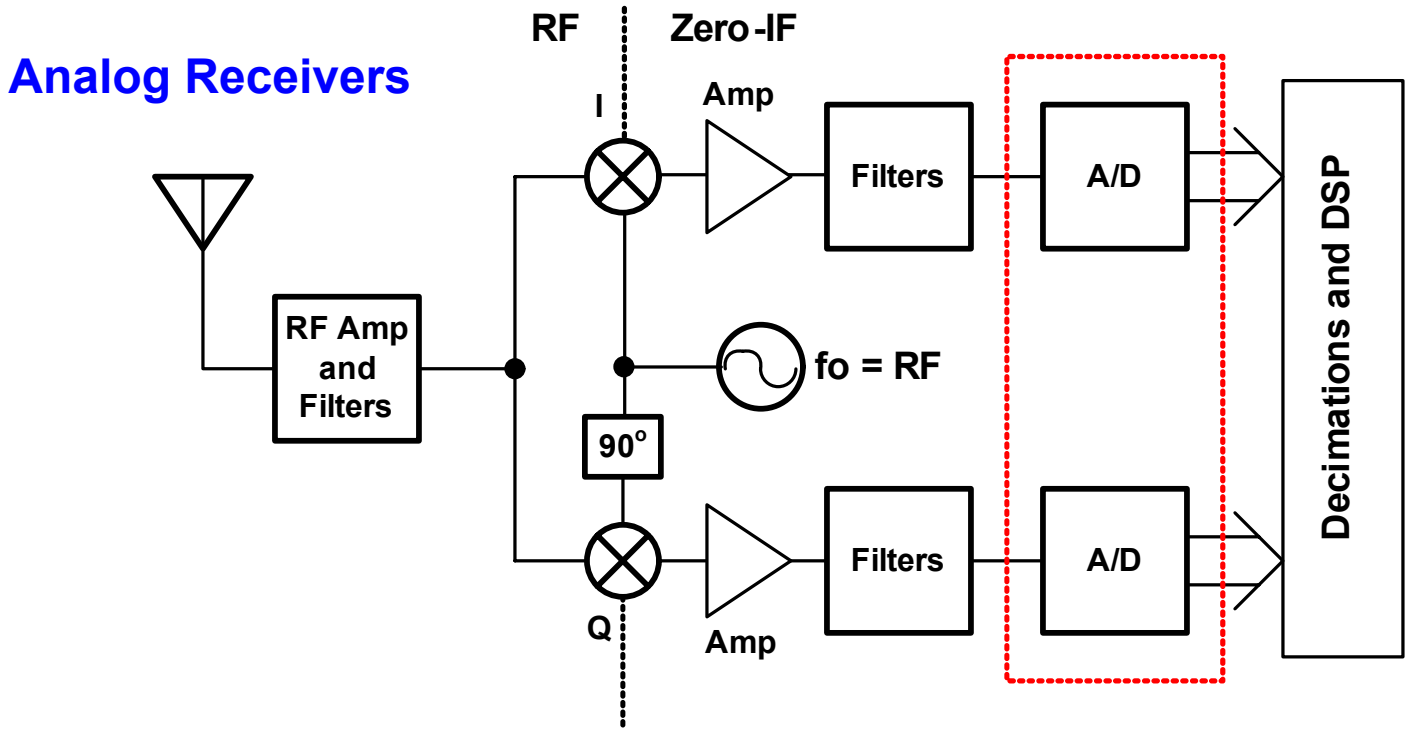


Fig. 2. Block diagrams of analog direct conversion receiver.

Ref: Stephen A. Jantzi et al. , IEEE Journal of solid-state Circuits,Vol.32, No. 12, September 1997

1.Introductions

1.2 Front - End Receiver Architectures: Direct Conversion

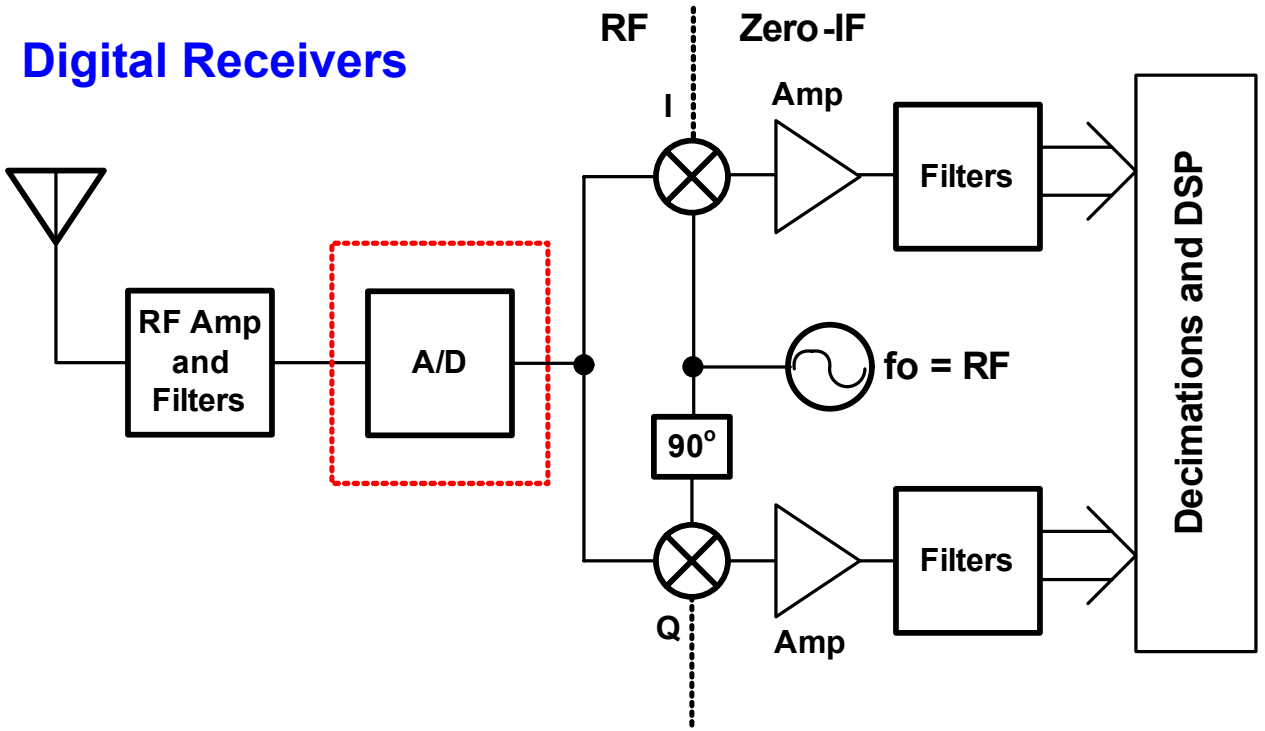


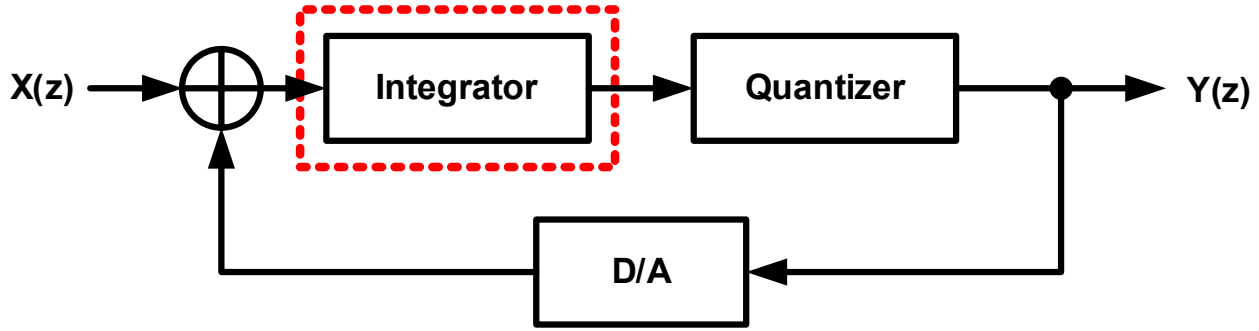
Fig. 3. Block diagrams of digital direct conversion receiver.

Ref. : Aarno Parssinen, Direct conversion receivers in wide-band system, KAP, 2001

1.Introductions

1.3 Sigma-Delta Analog-to-Digital Converters

(a) Low-Pass Sigma-Delta Modulations



(b) Band-Pass Sigma-Delta Modulations

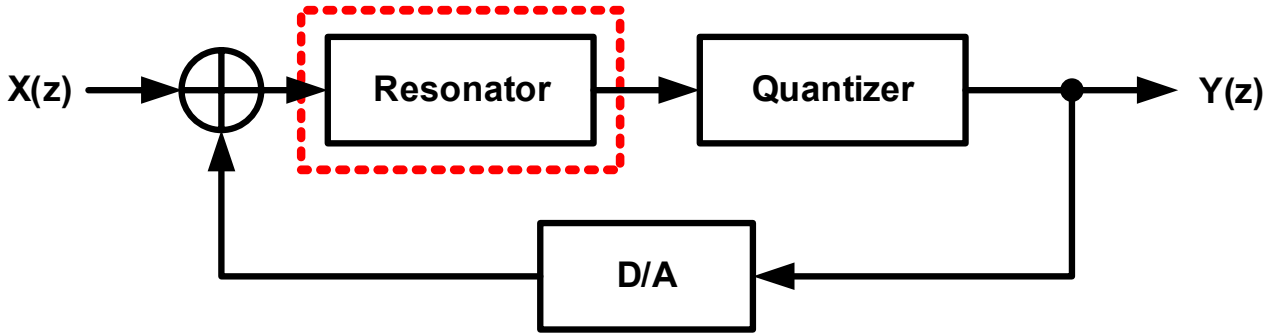


Fig. 4. Block diagrams of lowpass and bandpass sigma-delta modulations.

Ref. : J.M. de la Rosa et al., Microelectronics Journal 32(2001) 1017 - 1033

1.4 Conventional Switched-Capacitor (SC) Techniques

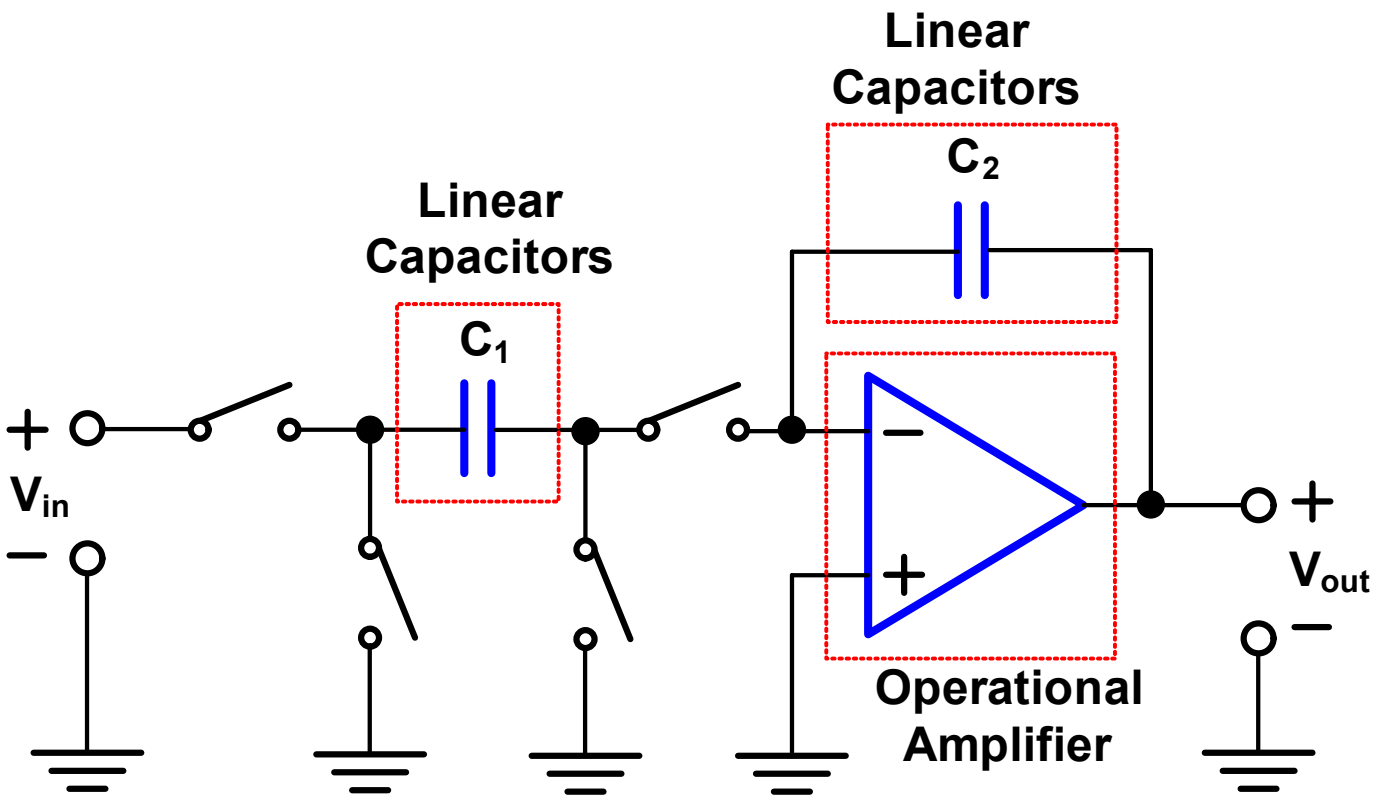
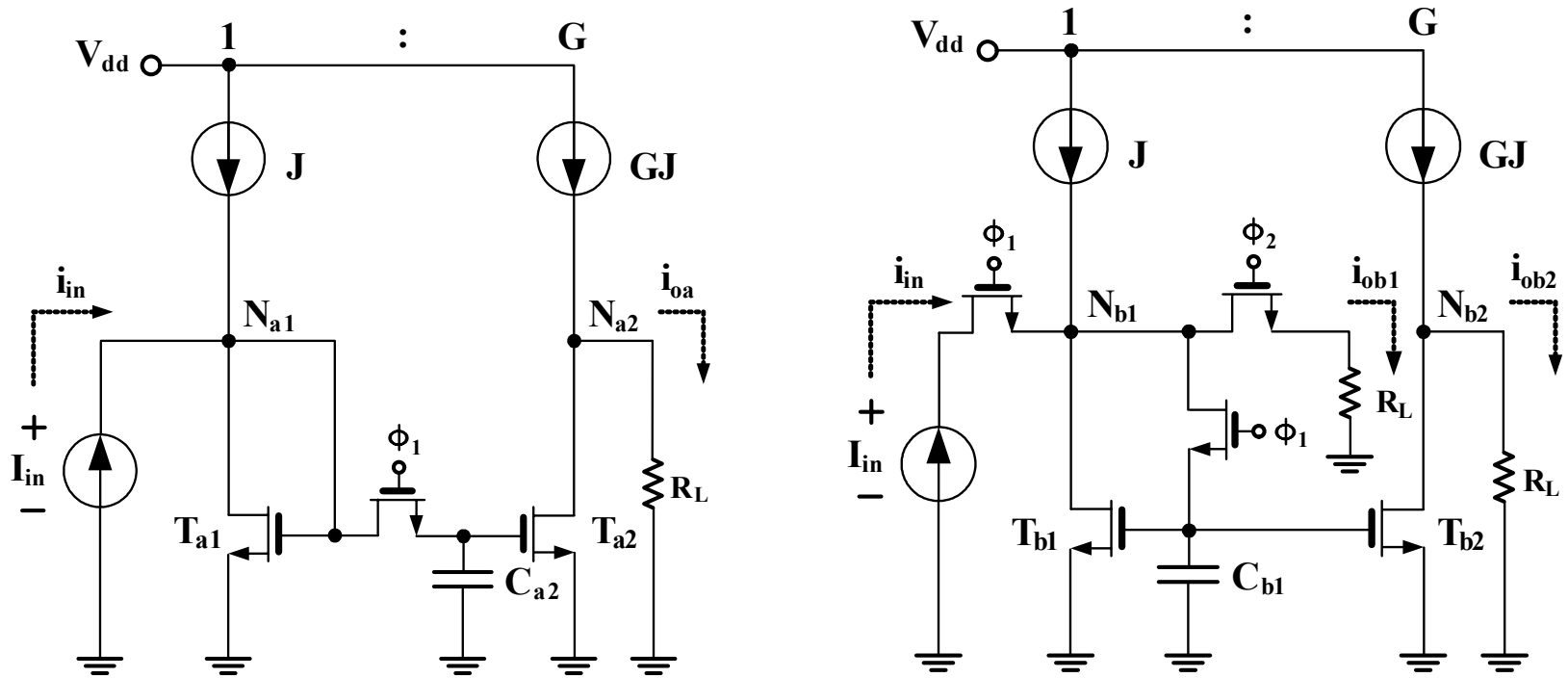


Fig. 5. The circuit diagram of a single-ended switched-capacitor integrator.

Ref. : Jen-Shuin et al. , IEICE Trans. FUNDAMENTALS,Vol.E87-A, No.2 FEBRUARY 2004

2. Existing Switched-Current Techniques and Primary Errors

2.1 Basic circuits utilizing class A configurations



First-Generation Second-Generation

Fig. 6. The circuit diagram of the first and second generation SI memory cells.

2. Existing Switched-Current Techniques and Primary Errors

2.2 Basic circuits utilizing class AB configurations

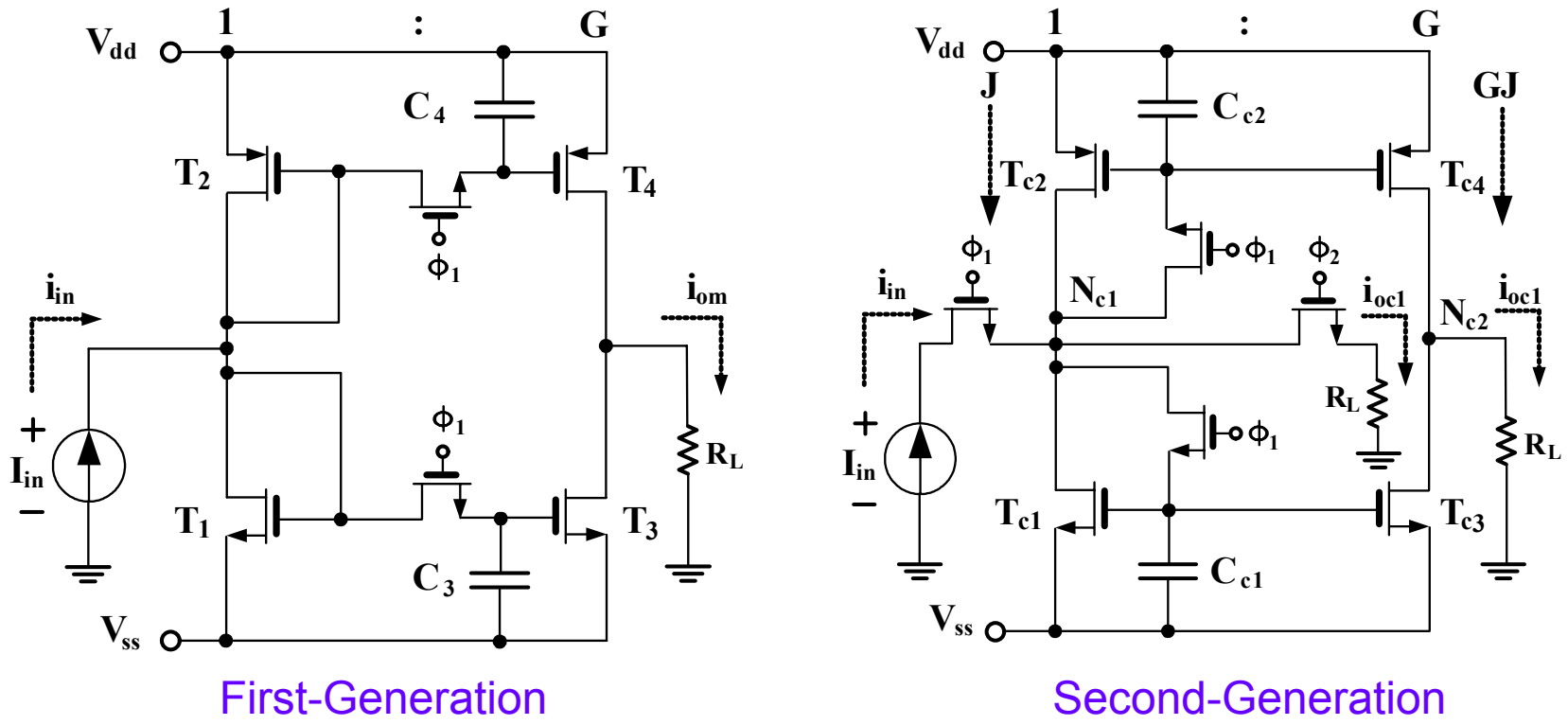


Fig. 7. The circuit diagram of a single-ended switched-capacitor integrator.

2. Existing Switched-Current Techniques and Primary Errors

2.3 Errors from mechanisms of memory switches

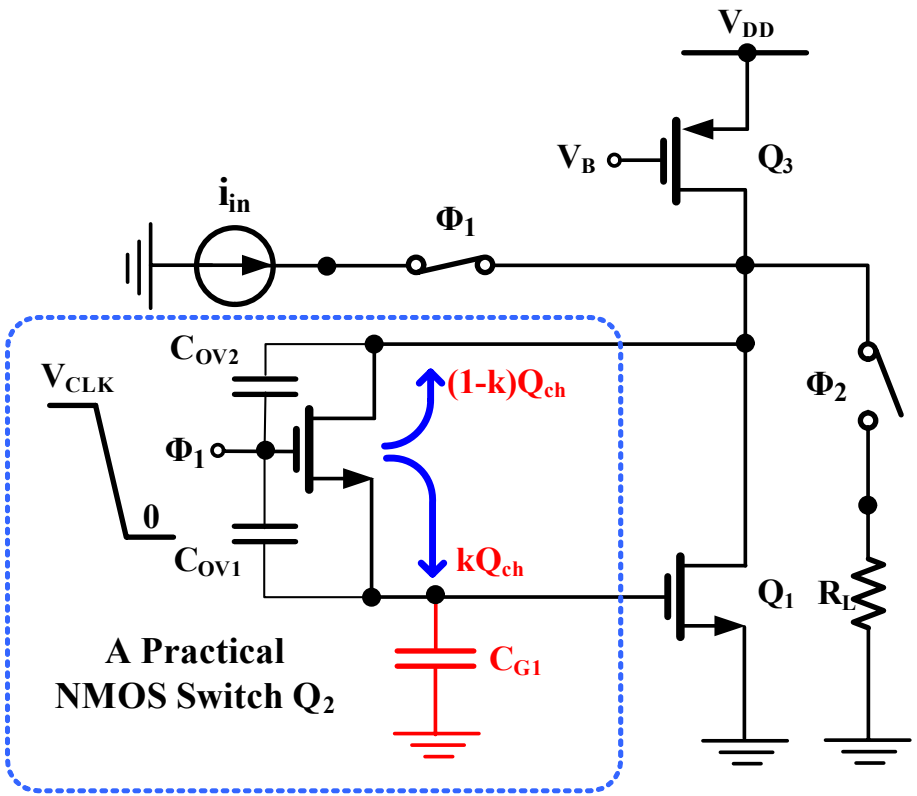


Fig. 8. The first generation class A SI memory cell demonstrating switching mechanisms.

Charge-Injection Errors

Channel charges in an inversion layer

$$Q_{ch} = W_2 L_2 C_{ox} (V_{gs2} - V_{T2}) \quad \text{... (1)}$$

Resulting error voltage

$$\delta v_1 = \frac{Q_{ch}}{kC_{G1}} \quad \text{... (2)}$$

$$\delta v_1 = \frac{W_2 L_2 C_{ox} (v_{GS2} - V_{t2})}{kC_{G1}} \quad \text{... (3)}$$

2. Existing Switched-Current Techniques and Primary Errors

2.4 Errors from mechanisms of memory switches

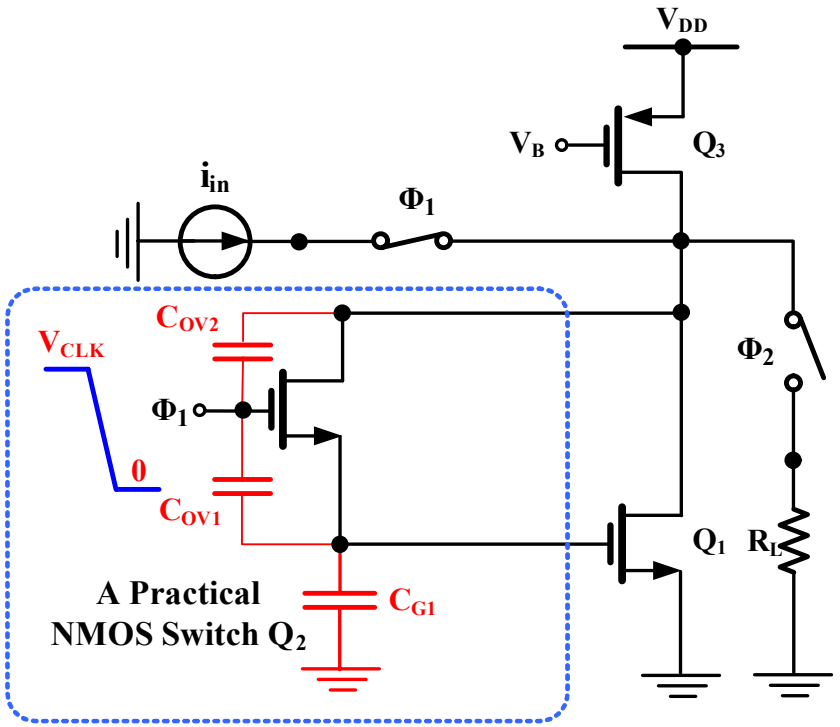


Fig. 9. The first generation class A SI memory cell demonstrating switching mechanisms.

Clock-Feedthrough Errors

The resulting error voltage

$$\delta V_2 = \left(\frac{C_{OV1}}{C_{OV1} + C_{G1}} \right) V_{CLK} \qquad \text{... (4)}$$

2. Existing Switched-Current Techniques and Primary Errors

2.5 Resulting error currents

The output current error

$$\delta i_{D1}[n+0.5] = k_1^{/}(\delta v)^2 + 2\sqrt{k_1^{/}}\,\delta v\sqrt{1+\frac{i_{in}[n]}{J}} \qquad \text{... (5)}$$

Taylor series analysis

$$\delta i_{D1}[n+0.5] = \delta i_{D1}^{/}[n+0.5] + \delta i_{D1}^{//}[n+0.5] \qquad \text{... (6)}$$

$$\delta I_{D1}^{/}[n+0.5] = \frac{k_n^{/} W_1}{2L_1}(\delta V)^2 + \delta V\sqrt{\frac{2Jk_n^{/} W_1}{L_1}} \qquad \text{... (7)}$$

$$\delta i_{D1}^{//}[n+0.5] = \delta V\sqrt{\frac{2Jk_n W_1}{L_1}}\left(\frac{i[n]/J}{2} - \frac{(i[n]/J)^2}{8} + \frac{(i[n]/J)^3}{16}\ldots\right) \qquad \text{... (8)}$$

2. Existing Switched-Current Techniques and Primary Errors

2.6 Conduction errors

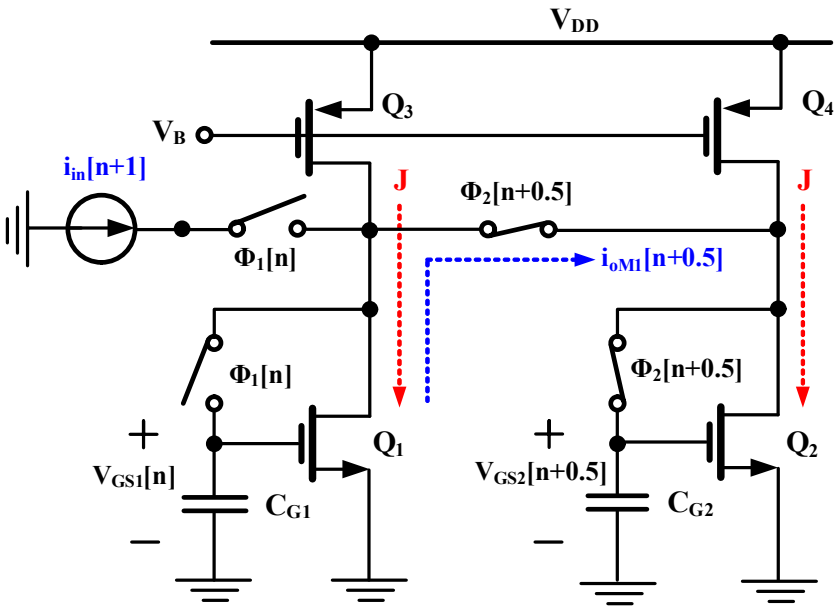


Fig. 10. Cascade connection of two memory cells.

Gate-source voltage at two phases

$$v_{GS1}[n] = \sqrt{\frac{(J + i_{in}[n])}{k_1}} + V_{t1} \quad \text{... (9)}$$

$$v_{GS2}[n + 0.5] = \sqrt{\frac{2(i_{in}[n] + J)}{k_1'}} + V_{t2} \quad \text{... (10)}$$

Total output conductance

$$g_{oM1} = g_{o1} + g_{o3} + \left(\frac{C_{GD1}}{C_{G1} + C_{GD1}}\right) g_{m1} \quad \text{... (12)}$$

The error current

$$\delta i_o[n + 0.5] = g_{m,eff}\left(v_{GS2}[n + 0.5] - v_{GS1}[n]\right) \quad \text{... (13)}$$

3. Proposed SI memory Cell

3.1 Block diagrams and two-phase Clock

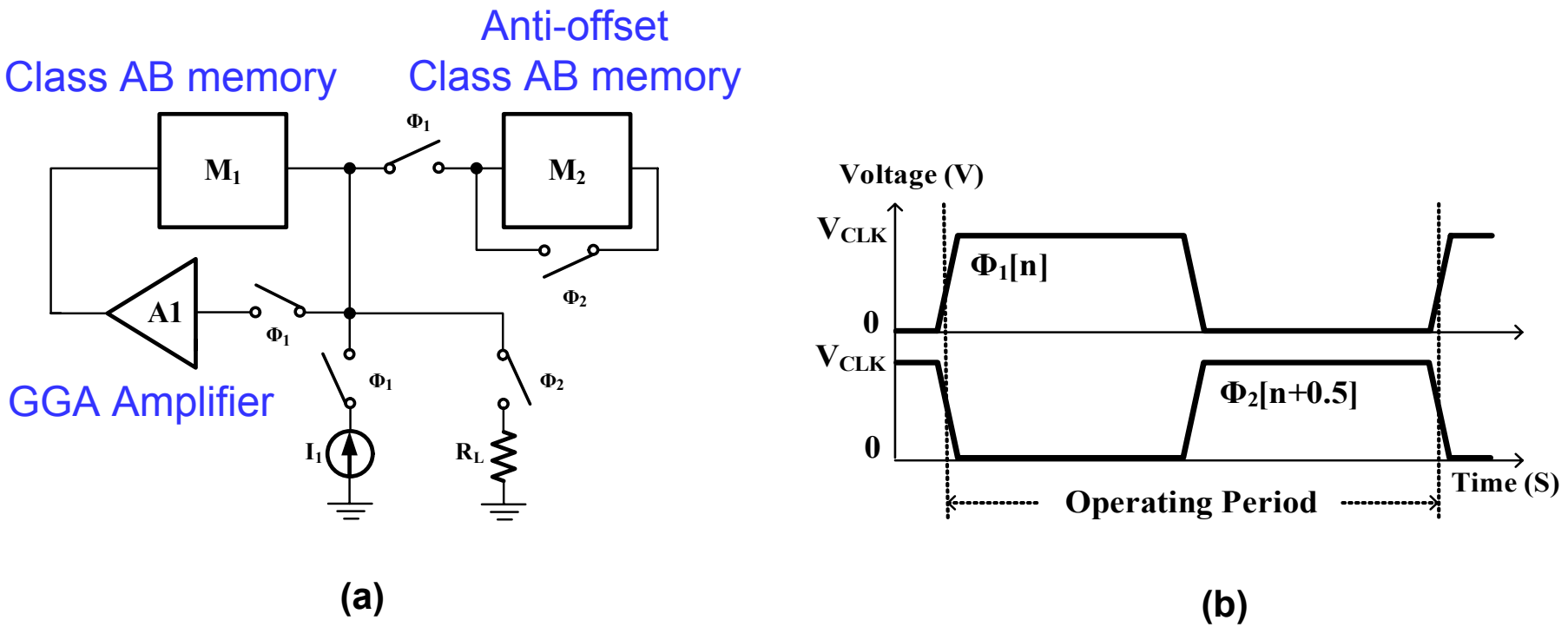


Fig. 11. (a) block diagrams and (b) two-phase clock of the proposed single-ended virtually grounded drain class AB SI memory cell.

3. Proposed SI memory Cell

3.2 Circuit configurations in transistor levels

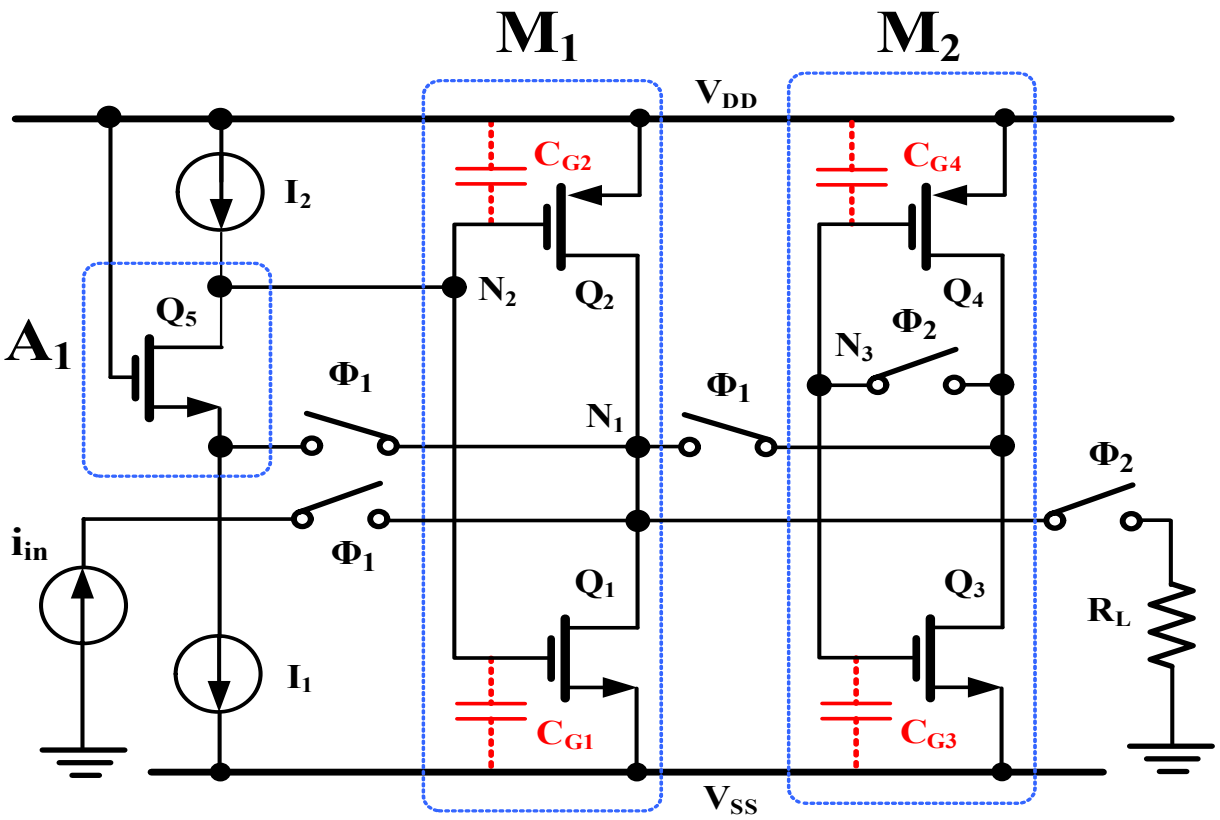


Fig. 12. circuit configurations the proposed single-ended virtually grounded drain class AB SI memory cell.

3. Proposed SI memory Cell

3.3 Circuit operations on the sampling phase

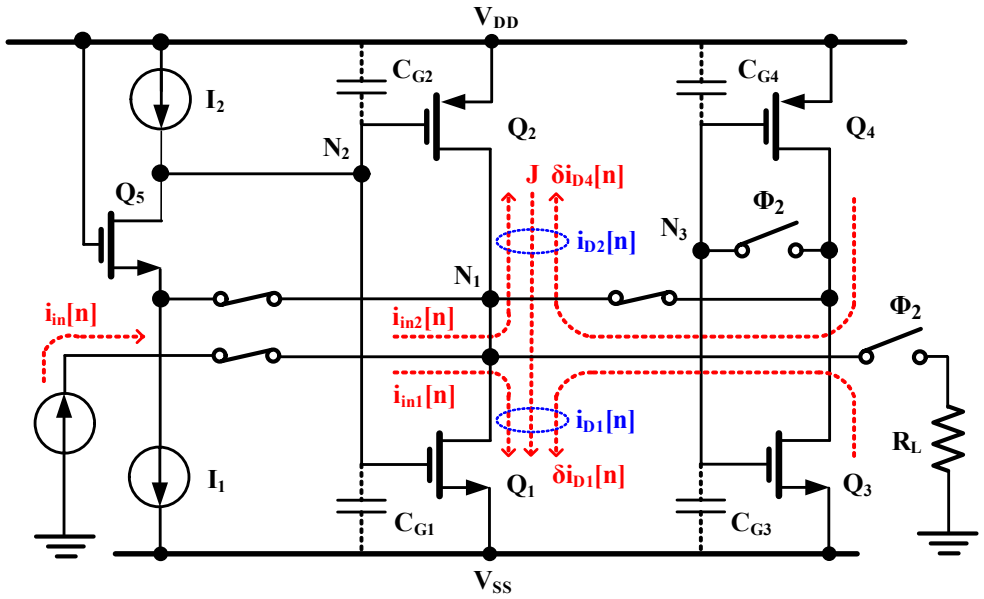


Fig. 13. Circuit operations on the sampling phase.

Voltage at the node N_2

$$v_{N2}[n] = Av_{N1}[n] \quad \text{... (14)}$$

Drain currents

$$i_{D1}[n] = J + \left(\frac{Ag_{m1}}{Ag_{m1} + g_{o1}}\right) i_{in1}[n] + \delta i_{D3}[n] \quad \text{... (15)}$$

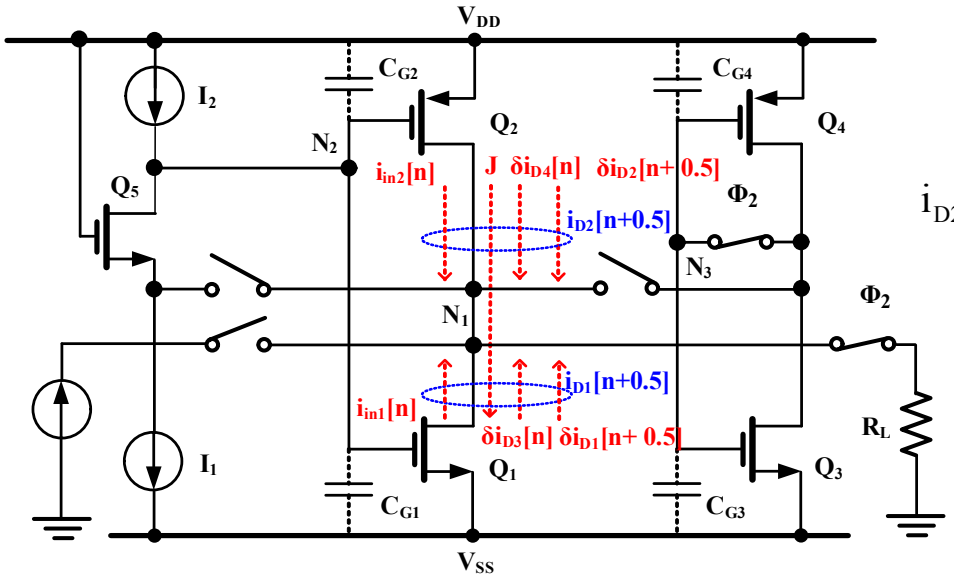
$$i_{D2}[n] = J - \left(\frac{Ag_{m2}}{Ag_{m2} + g_{o2}}\right) i_{in2}[n] - \delta i_{D4}[n] \quad \text{... (16)}$$

Voltage at the node N_1

$$V_{N1}[n] = V_{DD} + \left(\frac{i_{in}[n]}{Ag_{m1} + Ag_{m2} + g_{o1} + g_{o2}}\right) \quad \text{... (17)}$$

3. Proposed SI memory Cell

3.4 Circuit operations on the output phase



$$i_{D1}[n+0.5] = J - \left(\frac{Ag_{m1}}{Ag_{m1}+g_{o1}}\right) i_{i1}[n] - \delta i_{D3}[n] + \delta i_{D1}[n+0.5] \quad \text{... (18)}$$

$$i_{D2}[n+0.5] = J + \left(\frac{Ag_{m2}}{Ag_{m2}+g_{o2}}\right) i_{i2}[n] + \delta i_{D4}[n] - \delta i_{D2}[n+0.5] \quad \text{... (19)}$$

$$i_{D2}[n+0.5] = - \left(\frac{Ag_{m1}+Ag_{m2}}{Ag_{m1}+Ag_{m2}+g_{o1}+g_{o2}}\right) (i_{in1}[n] + i_{in2}[n]) \quad \text{... (20)}$$

Fig. 14. Circuit operations on the output phase.

3. Proposed SI memory Cell

3.5 z-Domain transformation

Table 2. Time domain and z-domain transformations.

Time-Domain	Z-Domain
$i_o[n + 0.5] = - i_{in}[n]$	$H(z)= \frac{I_o(z)}{I_{in}(z)} =- z^{-\frac{1}{2}}$

The output current is an inverted half-period delayed current sampled.

The current gain is ideally at unity.

Such transfer function is a basic function for implementing either integrator or resonator.

4. Simulation Results and Discussions

4.1 Simulation Environments

Table 3. The simulation process and parameters.

Parameters	Process or values
Technology	Alcatel Mietec 0.5 μm CMOS C05MD Technology
Power voltage supply	±0.8 V
The ambient temperature	26° C
The clock voltage signal V_{CLK} is	0 to 0.8 V
Bias current	6 μA (Memory) and 1 μm (Amplifier)
Aspect ratio of PMOS Memory	27μm /2 μm
Aspect ratio of NMOS Memory	15μm /4 μm
Aspect ratio of NMOS Amplifier	5μm /2 μm
Aspect ratio of NMOS Switches	0.8 μm/0.5 μm

4. Results and Discussions

4.2 Current gains

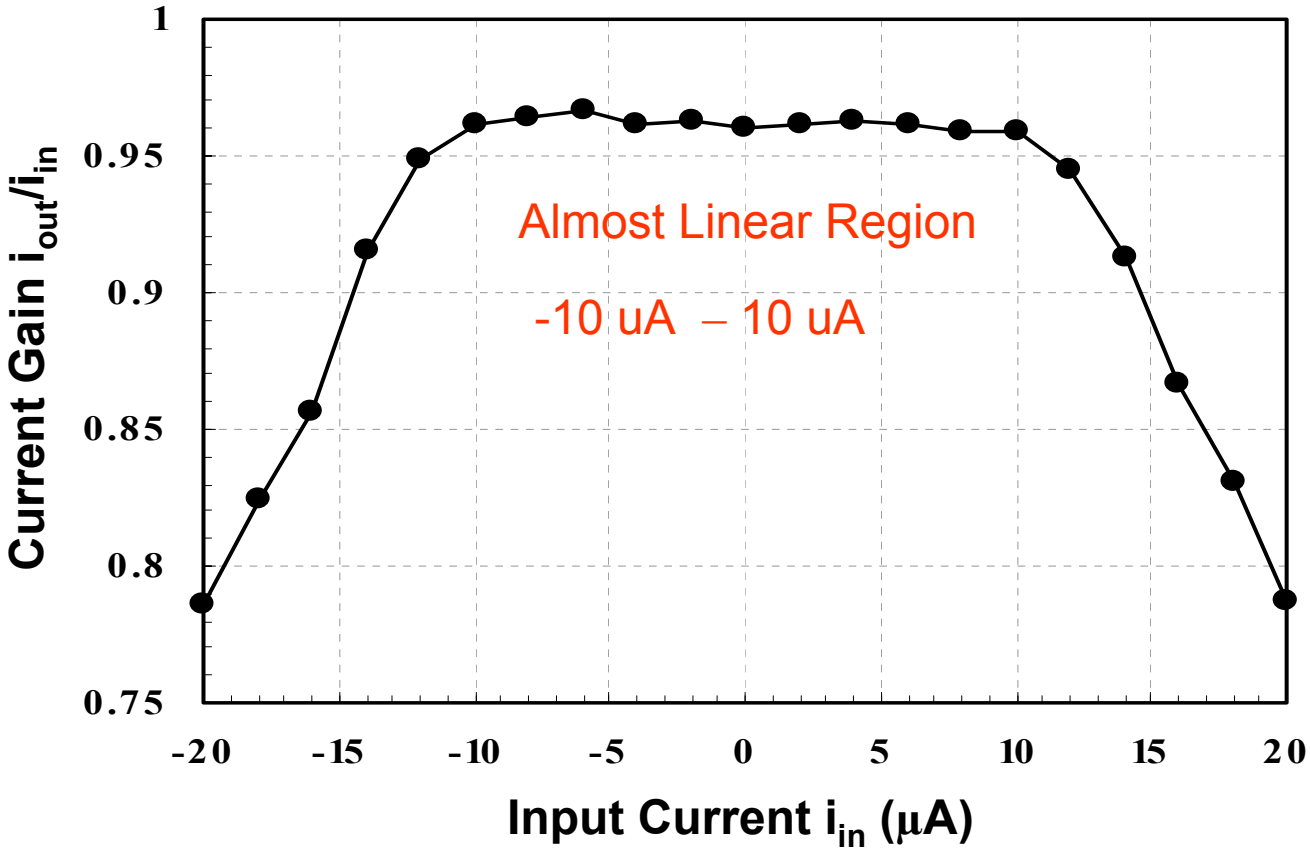
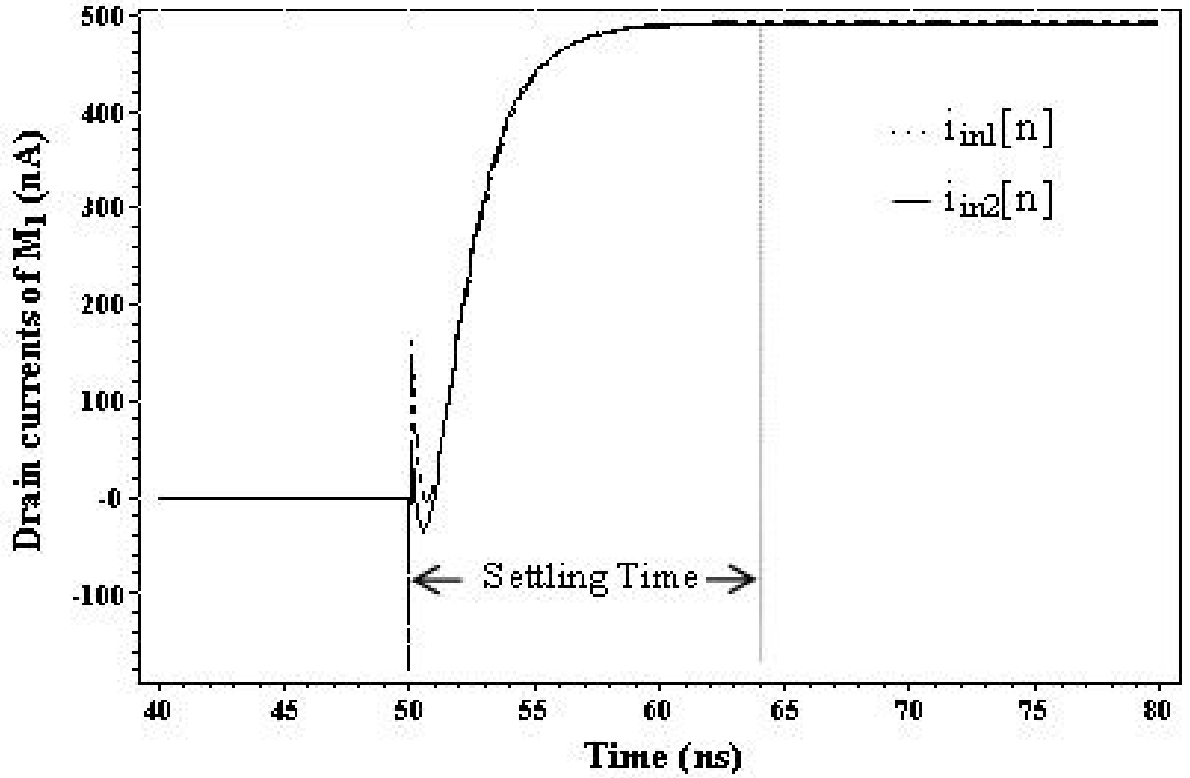


Figure 15. Plots of the current gain i_{out}/i_{in} versus the input current i_{in}.

4. Results and Discussions

4.3 Settling behaviors



The bias current is 6 uA.

The input current is 10 uA.

The settling time at 0.1% accuracy is approximately 14 ns.

The maximum useful sampling frequency is 70 MHz.

Equally settling behaviors of NMOS and NMOS memories are clearly observed.

Figure 16. Settling behaviors of the memory M_1 on the sampling phase $\Phi_1[n]$

4. Results and Discussions

4.4 Relative error currents

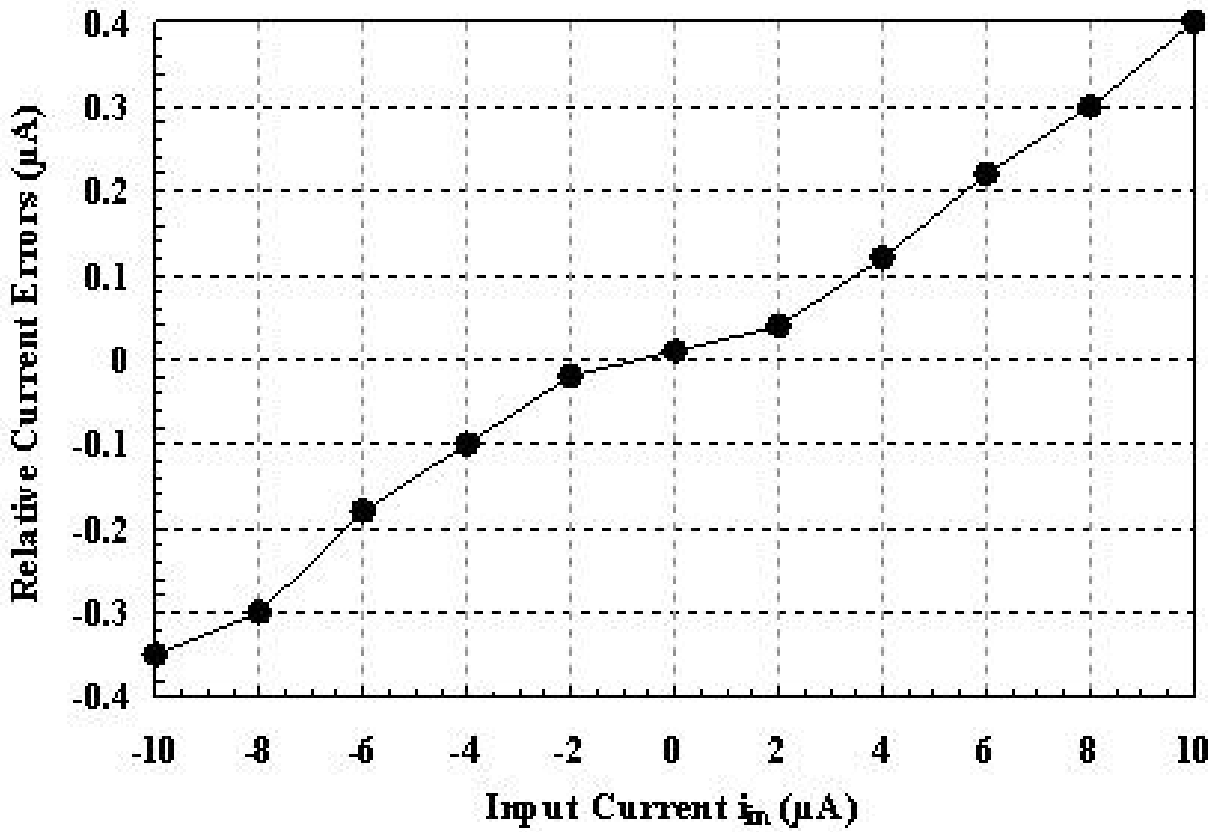


Figure 17. Plots of relative error currents of the memory cell versus input current signal.

4. Results and Discussions

4.5 Simulated input and output waveforms

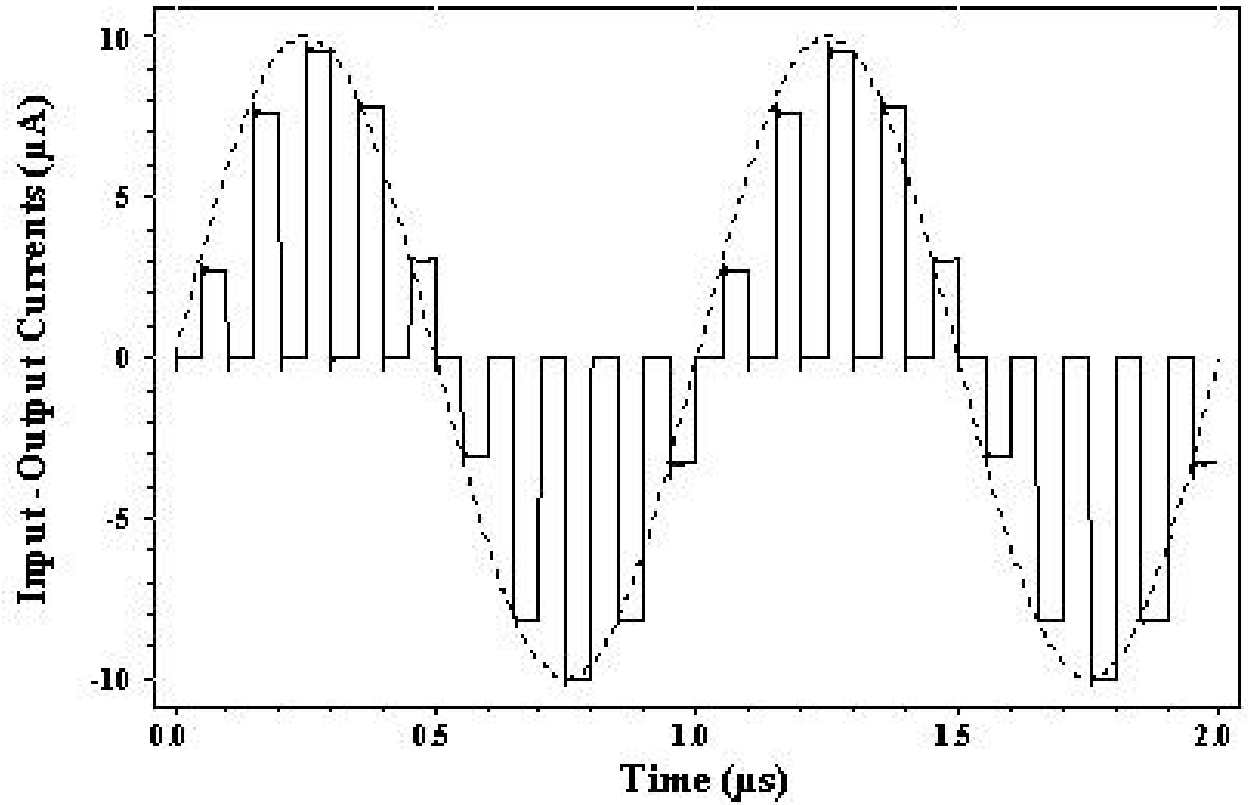


Figure 18. Sinusoidal input current and resulting sampled output current waveforms, using dotted and solid lines, respectively.

5. Conclusions

5.1 The single-ended virtually grounded drain class AB SI memory cell has been presented.

5.2 The technique is relatively simple based on (i) a single-ended virtually grounded drain class AB memory using a level shifted grounded gate amplifier and (ii) an anti-offset class AB cell.

5.3 The proposed circuit offers low charge-injection, clock-feedthrough and conduction errors.

5.4 The relatively complex differential configuration and multiple-step sampling are not required.

5.5 As a particular example, the proposed circuit possesses the low-power consumption of 20 mW and the maximum useful sampling frequency of 70 MHz.

5.6 The half-period delay sampled output current has been demonstrated.

5.7 The proposed circuit is a potentially alternative for low-power low-error switched-current sigma-delta modulation used in W-CDMA receivers.

6. Acknowledgements

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THANK YOU VERY MUCH