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Thai Microelectronics Center
Integrate Ideas Into Reality

Fabrication an Ultra-hydrophobic Surface with Low Reflectance by Using "Black Silicon" Structure

Presented by

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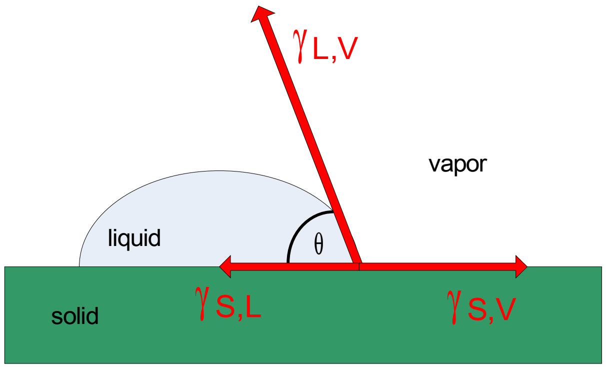
Superhydrophobic surface

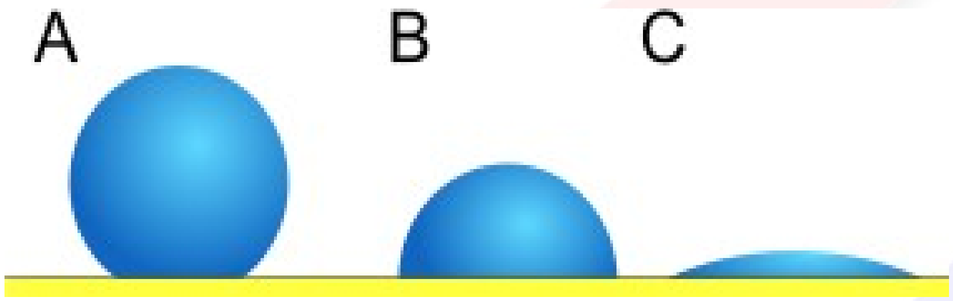


Water contact angle (WCA): The angle between the surface and the surface of a liquid droplet on the surface.

$$\cos\theta = \frac{\gamma_S - \gamma_{SL}}{\gamma_L}$$

contact angle < 90° → wettable surface

≥ 90° → non-wettable surface



θ ≥ 150° 149° ≥ θ ≥ 90° 90 ° > θ ≥ 0°

A→ superhydrophobic
B→ hydrophobic
C→ hydrophilic

Artifacts hydrophobic surface

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Techniques to make Superhydrophobic surfaces

Rough surface — low surface energy

Method to make a rough surface:

- **<u>Lithography and etching</u>**
- **Electrochemical reaction and deposition**
- **Mechanical abrasion**
- **Crystallization control**

Low surface energy materials:

- **Fluorocarbons:** Teflon, PFOS, etc.
- **<u>Silicones: TPFS, PDMS , SFS</u>**
- **Organic materials:** PE, PS, polyamide, etc.
- **Inorganic materials:** ZnO, TiO_2

TPFS: trichloro(1H,1H, 2H,2H-perfluorooctyl)silane
PDMS: Polydimethylsiloxane
SFS: Semiflourinate silane

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Limitation of current technologies

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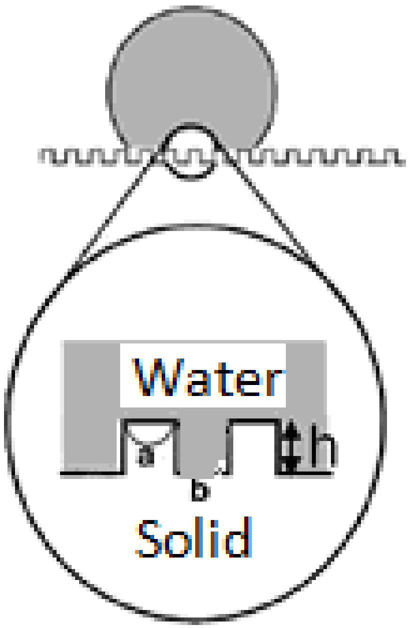
Wenzel



$$r = \frac{A_p + A_f}{A_f} = 1 + \frac{A_p}{A_f}$$

$$COS\theta_w = \frac{r(\gamma_S - \gamma_{SL})}{\gamma_L} = r\cos\theta_y$$

When,
r is the surface roughness factor, which is the ratio of the actual area of the rough surface to the projected area.
A_p is the surface area of pillar.
A_f, is the flat surface area

To reach the superhydrophobic surface;
1)Pillar size **(a, b) must be smallest** [max packing factor (P), max(a/b)] → Limitation of Lithography's resolution (0.5 µm).
2)Pillar height **(h) must be tallest** [max. aspect ratio (A.R.), max(h/a)] → DRIE etching tool's limit (10:1).
3)Coating materials **[cose$_y$ = -1]** → PDMS (-0.3528).

Beyond the current technology

Based on the limitation of lithography and etching tools. TMEC found the new method to make a nano-pillar structure without using patterning process.

This structure is called "Black Silicon"!!.

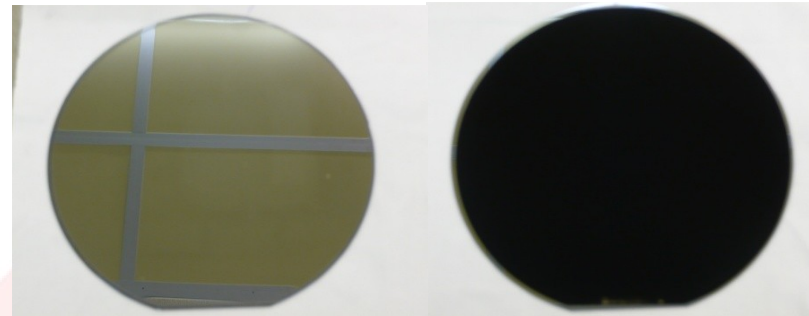
Black Silicon nano-structures

Black silicon was discovered in Eric Mazur's laboratory at Harvard University in 1988, as an unwanted side effect of reactive ion etching (RIE).

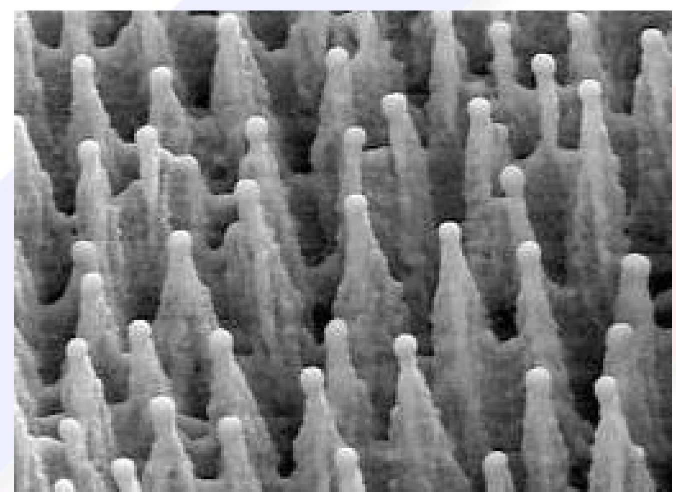
It is a semiconductor material. This surface modification of silicon has very low reflectivity and correspondingly high absorption of visible and infrared light.

Black silicon is a needle-shaped surface structure where needles are made of single-crystalline silicon and have a height above 10 µm, and diameter <1µm.

Black silicon can alternatively be used to make hydrophobic surfaces.



Bare Si	Black Si

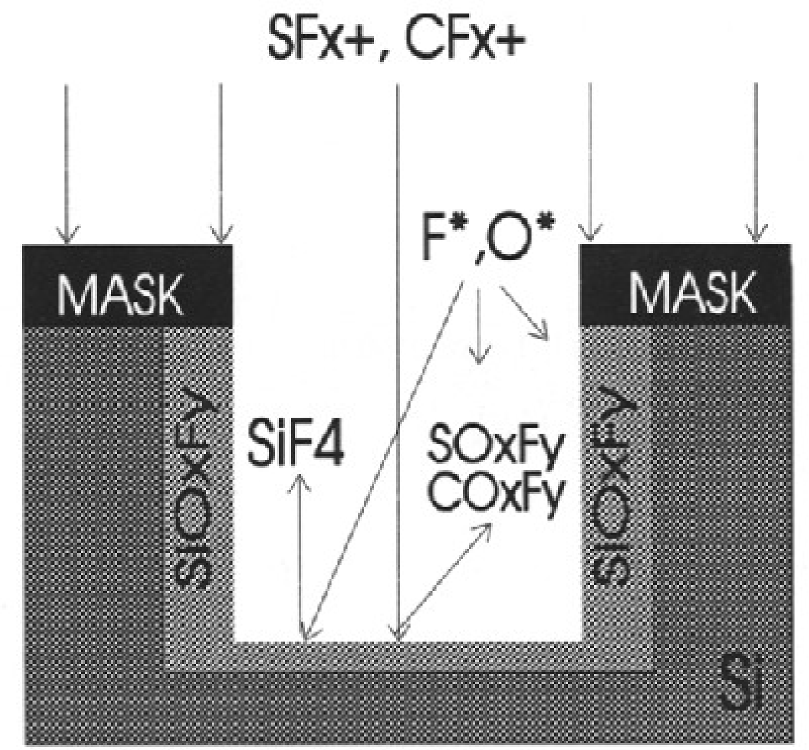


SEM image of Black Si

Black Silicon formation

In $SF_6/O_2/CHF_3$ RIE plasma process, SF_6 produces the F* radicals for the chemical etching of the Si, forming the volatile SiF_4. O_2 creates the O* radicals to passivate the Si surface with SiO_xF_y, and CHF_3 (or SF_6) is the source of CF_x+ (or SF_x+) ions, responsible for the removal of the SiO_xF_y layer at the bottom of the etching trenches forming the volatile CO_xF_y (or SO_xF_y).

At the same moment, native oxide and dust will act as micro masks and, because of the directional etching, spikes will appear. These spikes consist of a silicon body with a thin passivating siliconoxyfluoride skin.



Ref. *H. Jansen et al. I Microelectronic Engineering 27 (1995) 475-480*

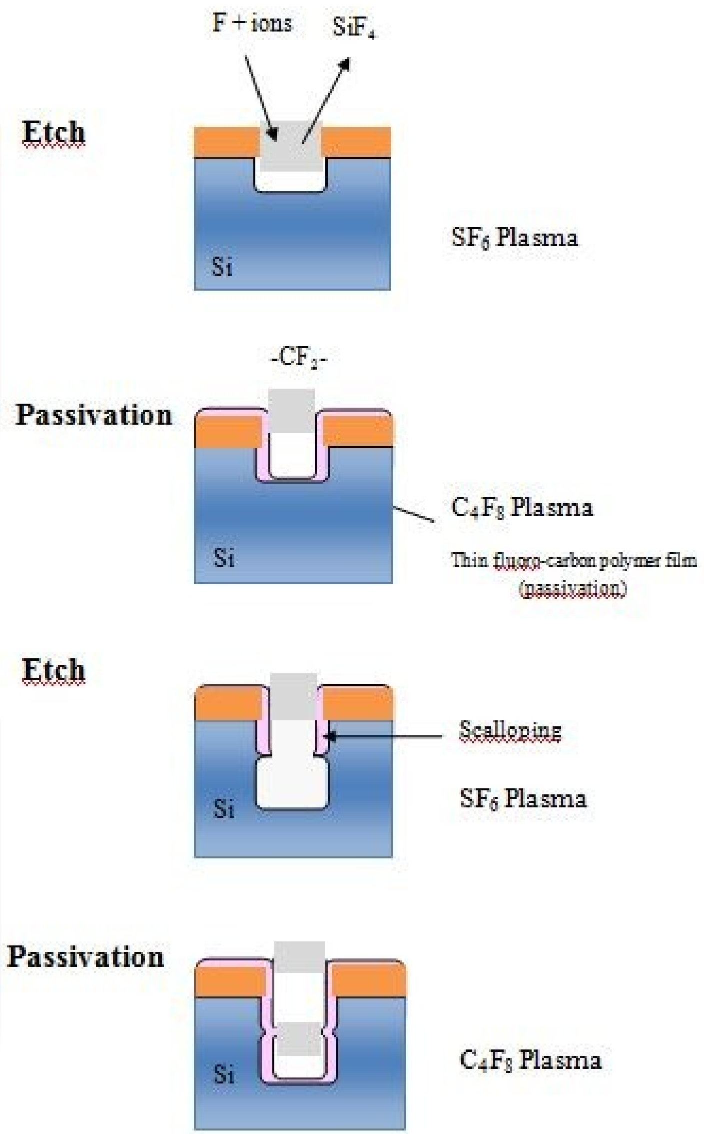
Black Silicon formation (Con't)

The height of the black Si pillar can be increases by using a Deep Reactive Ion Etching (**DRIE**) with **Bosch process**.

DRIE is a highly **anisotropic etch** process used to create deep, steep-sided holes and trenches in wafer. This concept use **multiple cycles of alternating etches and depositions**.

For the etch step, the wafer is attack by **SF_6** ions contained in the plasma.

For the deposition step, the wafer is deposited by **C_4F_8** to protect the sidewalls during each etch step.



Objective

To fabricate a nano-pillar structure without using patterning process, which has a ***superhydrophobic surface and low reflectance properties*** by using a "**Black silicon**" nano-structures.

Experimentals

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- DOE#1 was etched by RIE+DRIE Bosch's process.
- DOE#2 and DOE#3 were etched by only RIE process. (DOE#2 RF power < DOE#3 RF power)
- DOE#4 was etched by only DRIE Bosch's process.

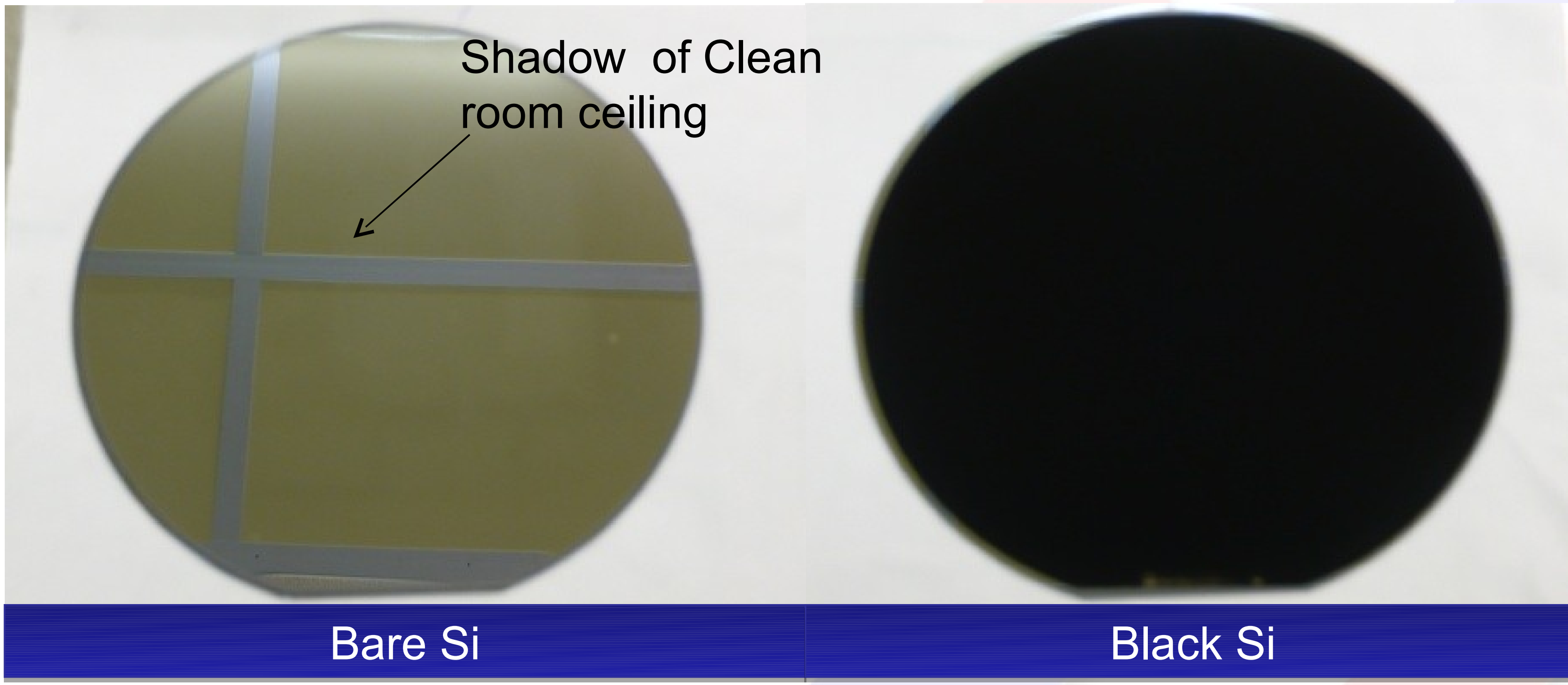
** Bosch etching loop is 27 loops.

Then, the samples were coated with trichloro(1H,1H, 2H,2H-perfluorooctyl)silane (TPFS) and baked at 120 ˚C for 1 hrs.

		Gas flow rate (sccm)				Energy (Watt)				
Condition	Process step	CF_4	SF_6	O_2	He	RF	ICP	Valve angle (Degrees)	Pressure (mTorr)	Process time (Second)
1	RIE etching	-	20	60	10	15	2000	35	23.5	15
	Bosch deposition	200	-	-	10	10	2000	50	18.0	8
	Bosch etching	-	150	-	10	15	2000	50	18.0	5
2	RIE etching	-	20	60	10	15	2000	35	23.5	15
3	RIE etching	-	20	60	10	40	2000	35	23.5	15
4	Bosch deposition	200	-	-	10	10	2000	50	18.0	8
	Bosch etching	-	33	100	10	15	2000	50	13.0	5

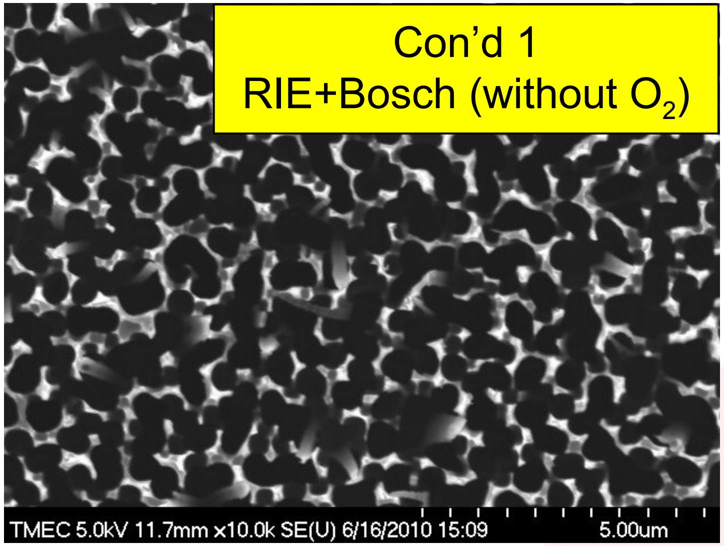
Tool: Plasma lab 100 from Oxford Instrument

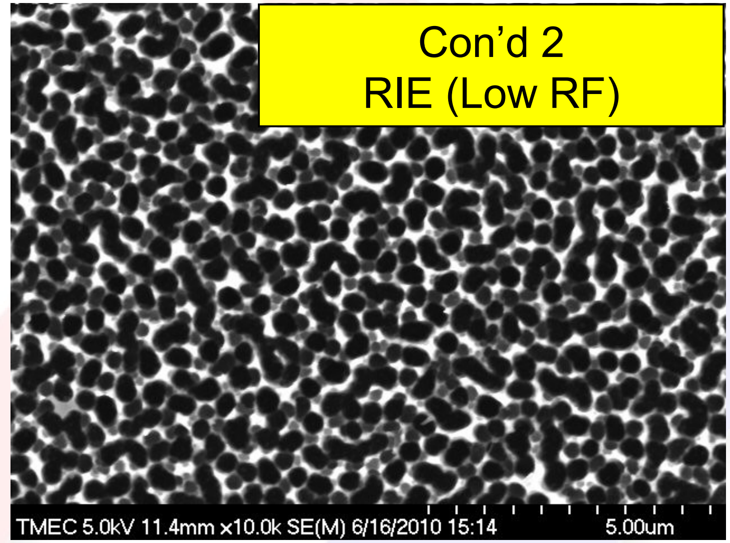
Black Silicon nano-structures

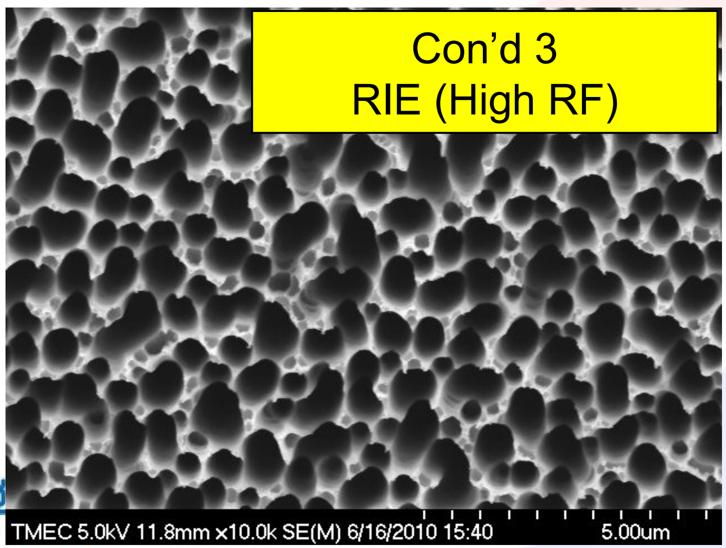


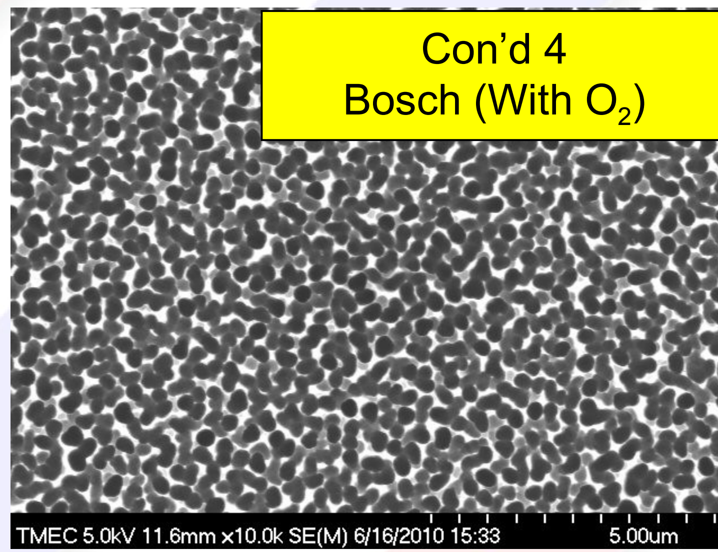
Black Silicon nano-structures (Top-view)

OM images shown Black silicon is a porous-liked structure.

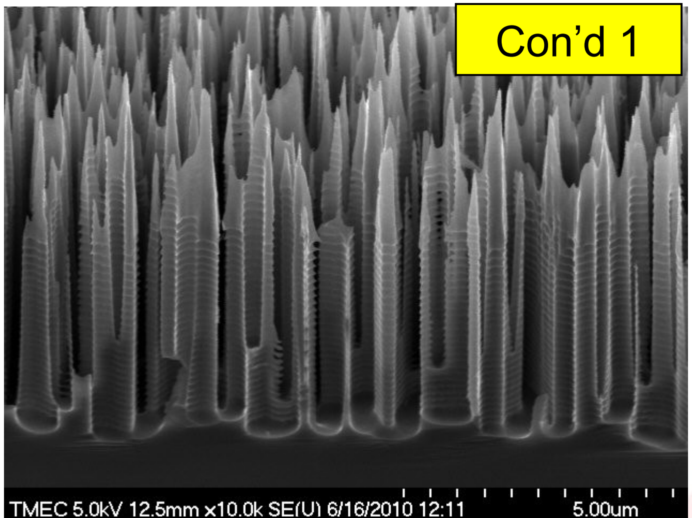




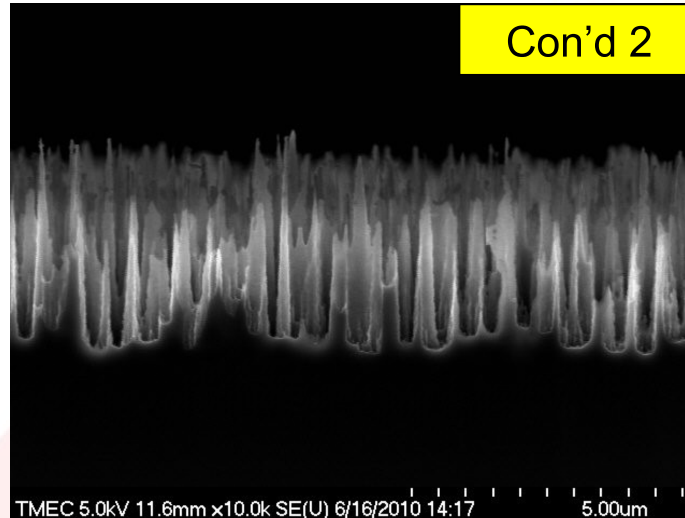




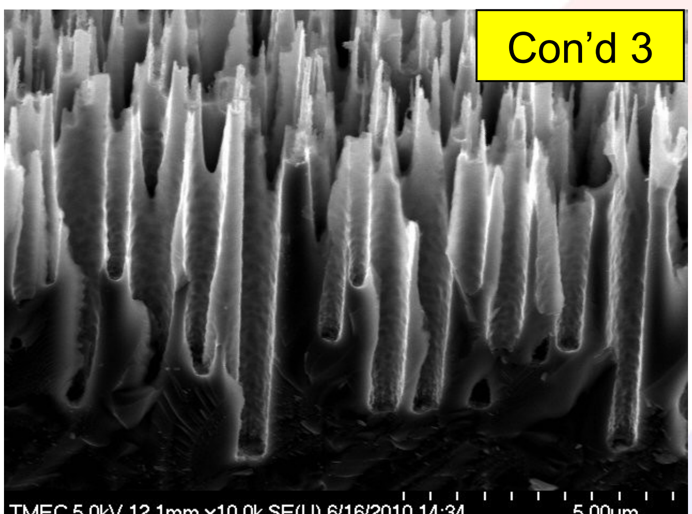
X-view SEM images



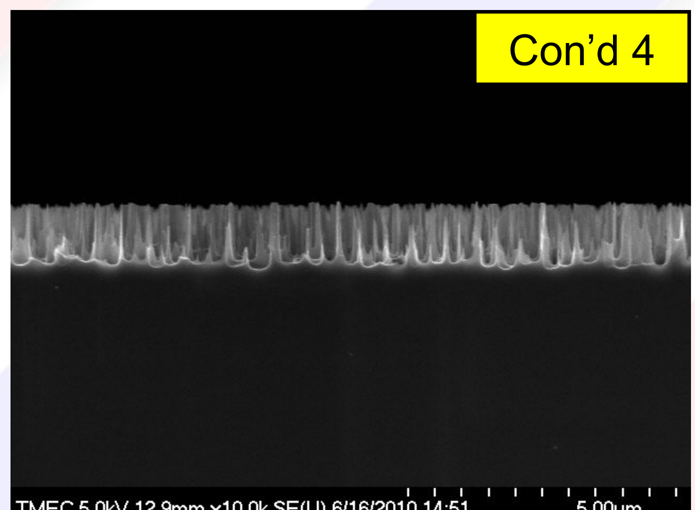
A= 250nm, h=7um, A.R.=28



A= 250nm, h=3.6um, A.R.=14.4

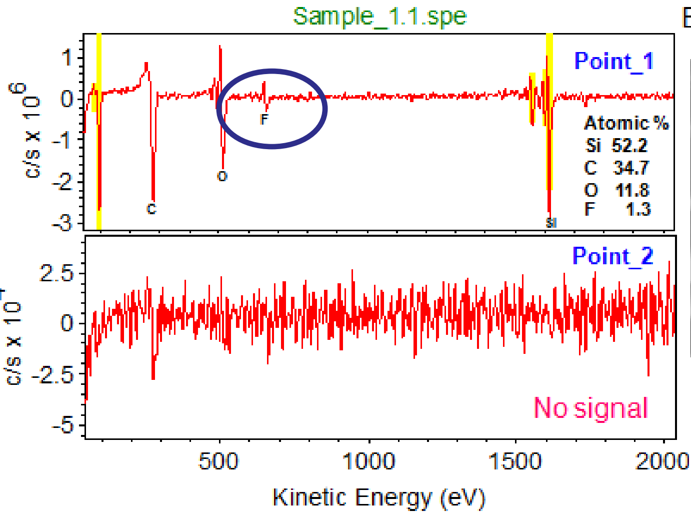


A= 250nm, h=4.07um, A.R.=16.3

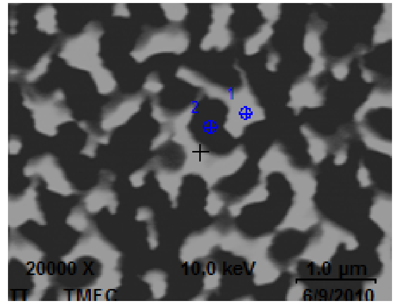


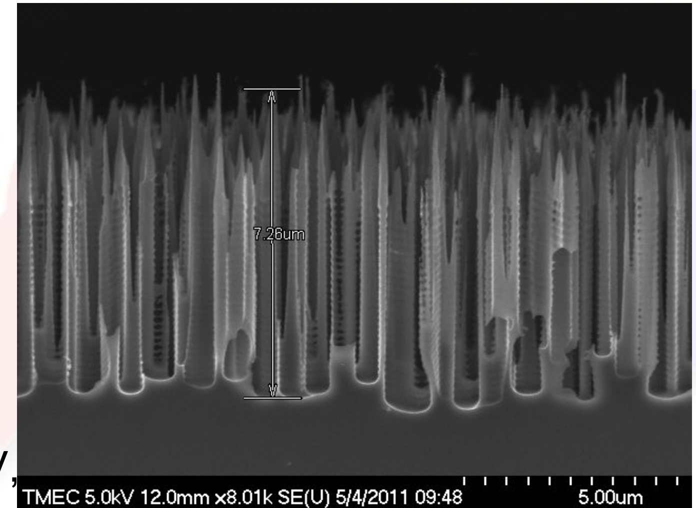
A= 113nm, h=1.15um, A.R.=0.45

AES spectrum for Black Si+Bosch etching (DOE#1)



Electron beam setting 10kV 10nA





Black Si 1
Depth: 7.26 um

AES condition:
10kV, 10nA, 40-2040eV, Tilt 0˚, Res. 1eV/step.

DRIE condition: 27 loops.	Bosch process trench etch.
1.Depth time = 8 sec.	1.Etch time = 5 sec.
2.Pressure = 18 Torr	2.Pressure = 18 Torr
3.Valve angle 50 deg.	3.Valve angle 50 deg.
4.CF_4 flow = 200 sccm.	4.CF_4 flow = 0
5.SF_6 flow = 0 sccm.	5.SF_6 flow = 150 sccm.
6.O_2 flow = 0 sccm.	6.O_2 flow = 0 sccm.
7.He flow = 10 sccm.	7.He flow = 10 sccm.
1.RF power = 10 Watt	**1.RF power = 15 Watt**
1.ICP power = 2000 Watt.	1.ICP power = 2000 Watt.
1.DC bias = 0 V.	**1.DC bias = 0 V.**

The "black region" is the silicon etched surface (Bare Si), and the "White region" is the Black Si pillar. The black silicon from DOE#1 has a Si, C, O, and F elements on the surface. The fluorine radical (F*) is a by-product from etching gas (SF_6 and CF_4).

AES spectrum for Black Si (DOE#2)

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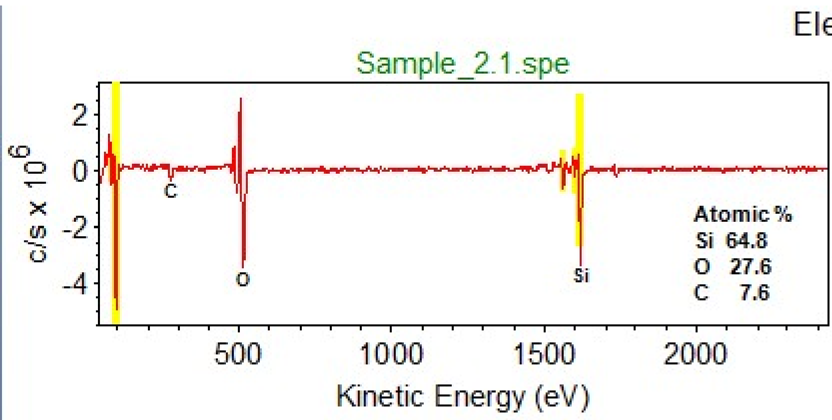
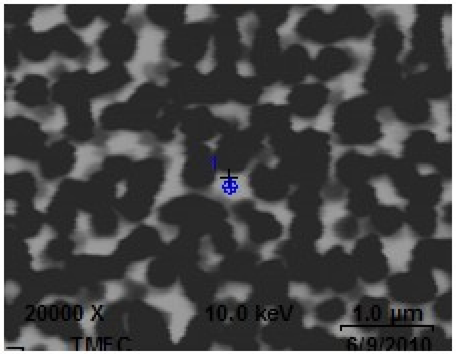
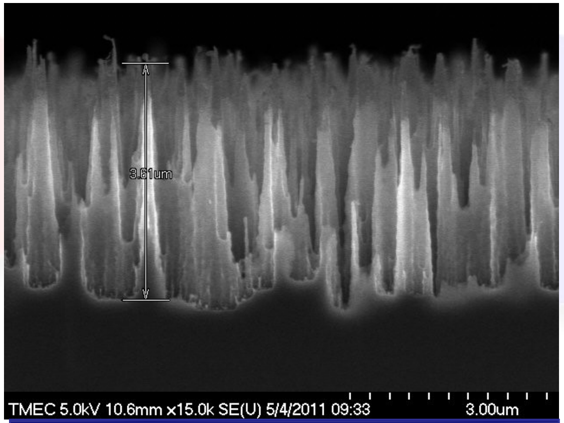


Electron beam setting 10kV 10nA





Black Si 2
Depth: 3.61 um

DRIE condition:
Etch only Black Si.
1.Etch time 15 sec.
2.Pressure = 23.5 Torr
3.Valve angle 35 deg.
4.CF_4 flow = 0
5.SF_6 flow = 20 sccm.
6.O_2 flow = 60 sccm.
7.He flow = 10 sccm.
1.RF power = 15 Watt
1.ICP power = 2000 Watt.
2.DC Bias = 117 v.

AES condition:
10kV, 10nA, 40-2040eV, Tilt 0˚, Res. 1eV/step.

AES results shown that there are only Si, O, and C as a component for the pillar in white region. It didn't have any "Flourine" thin film coated on the pillar sidewall. This may because there was not a "deposition step" during a RIE process, or the RF power is too low.

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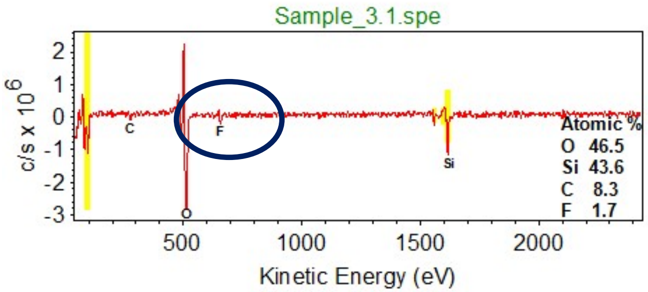
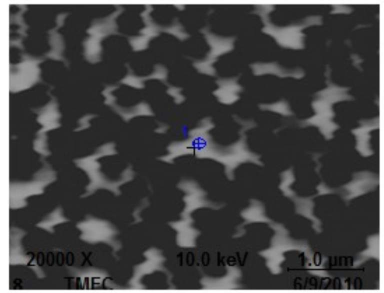
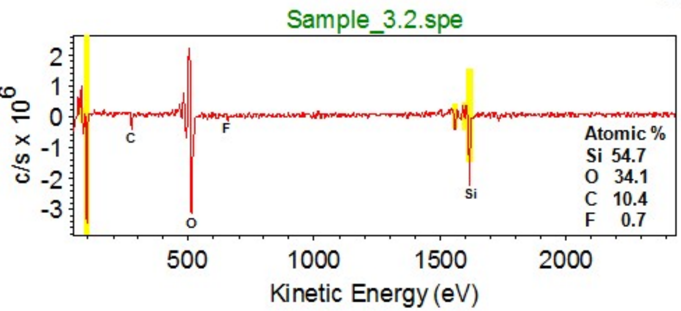
AES spectrum for Black Si (DOE#3)

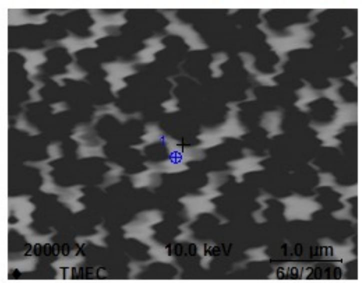
Electron beam setting 10kV 10nA

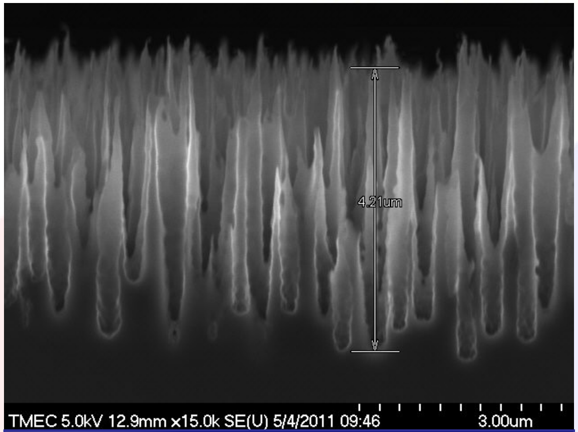




Electron beam setting 10kV 10nA







Black Si 3
Depth: 4.21 um

AES condition:
10kV, 10nA, 40-2040eV, Tilt 0˚, Res. 1eV/step.

DRIE condition:
Etch only Black Si.

1. Etch time 15 sec.
2. Pressure = 23.5 Torr
3. Valve angle 35 deg.
4. CF_4 flow = 0
5. SF_6 flow = 20 sccm.

1. O_2 flow = 60 sccm.
2. He flow = 10 sccm.

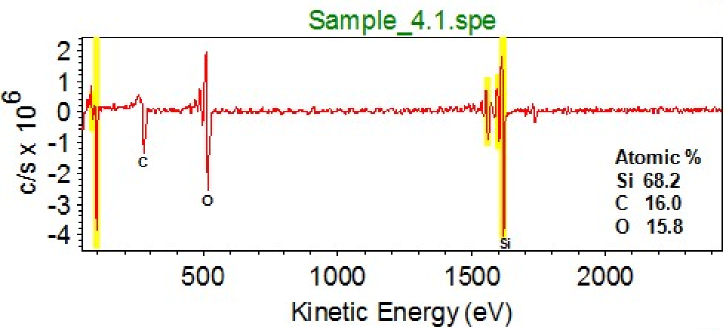
1.RF power = 40 Watt

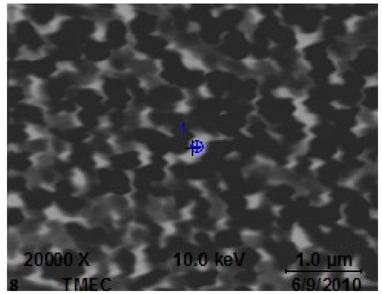
1. ICP power = 2000 Watt.
2. DC Bias = 117 v.

AES results shown that there are Si, O, F, and C as a component for the pillar in white region. When compared to Black Si2, the etch depth has increases when the RF power has increases. Moreover, there is some "Fluorine" deposited on the black Si pillar.

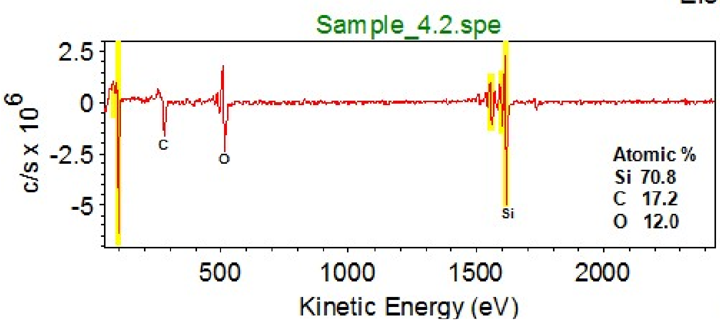
AES spectrum for Black Si+Bosch etching (DOE#4)

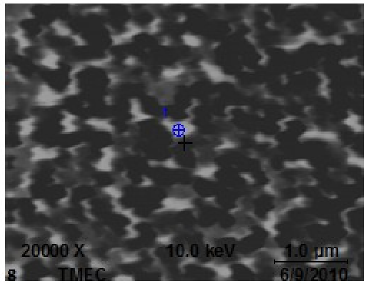
Electron beam setting 10kV 10nA

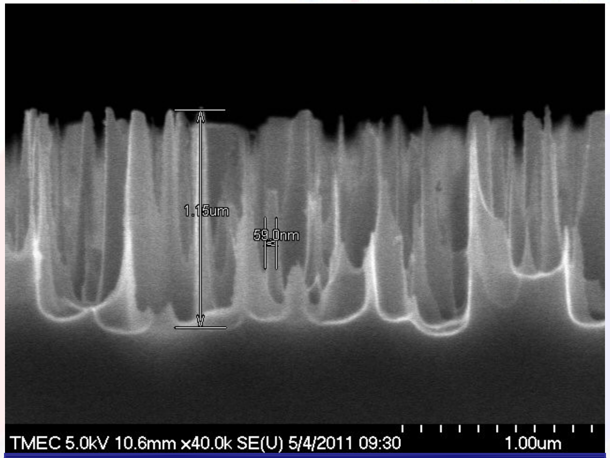




Electron beam setting 10kV 10nA







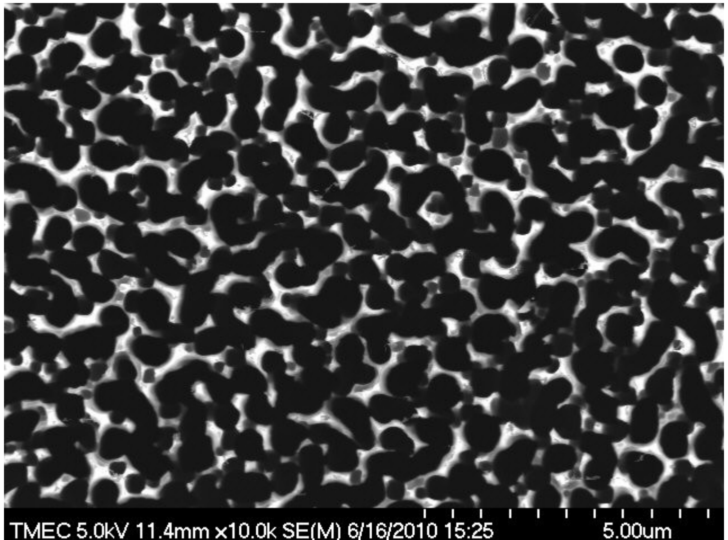
Black Si 4
Depth: 1.15 um

DRIE condition: 27 loops.
1.Depth time = 8 sec.
2.Pressure = 18 Torr
3.Valve angle 50 deg.
4.CF_4 flow = 0
5.SF_6 flow = 0 sccm.
6.O_2 flow = 0 sccm.
7.He flow = 10 sccm.
1.RF power = 10 Watt
1.ICP power = 2000 Watt.
1.DC bias = 0 V.

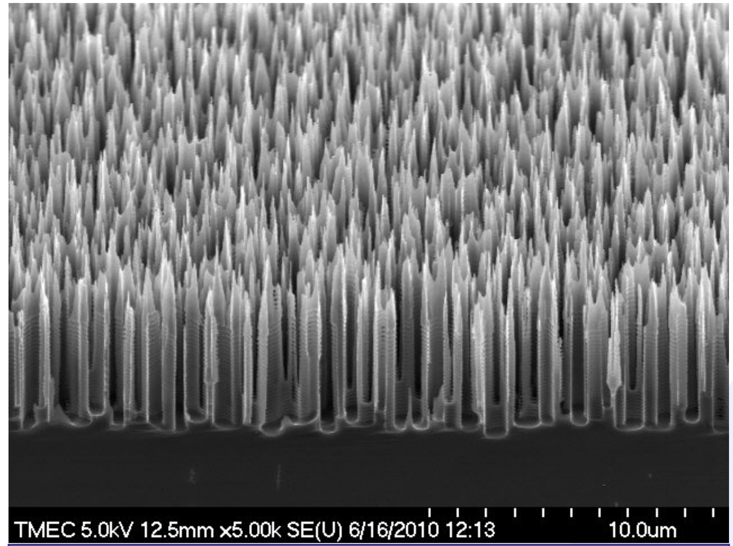
Bosch process shallow etch.
1.Etch time = 5 sec.
2.Pressure = 13 Torr
3.Valve angle 50 deg.
4.CF_4 flow = 0
5.SF_6 flow = 33 sccm.
6.O_2 flow = 100 sccm.
7.He flow = 10 sccm.
1.RF power = 15 Watt
1.ICP power = 2000 Watt.
1.DC bias = 0 V.

AES results shown that there are Si, O, and C as a component for the pillar in white region. It didn't have any fluorine on the pillar. When compared to DOE#1, the etch depth is very shallow because it didn't have a Bosch process.

SEM images after coated with TPFS (DOE#1)

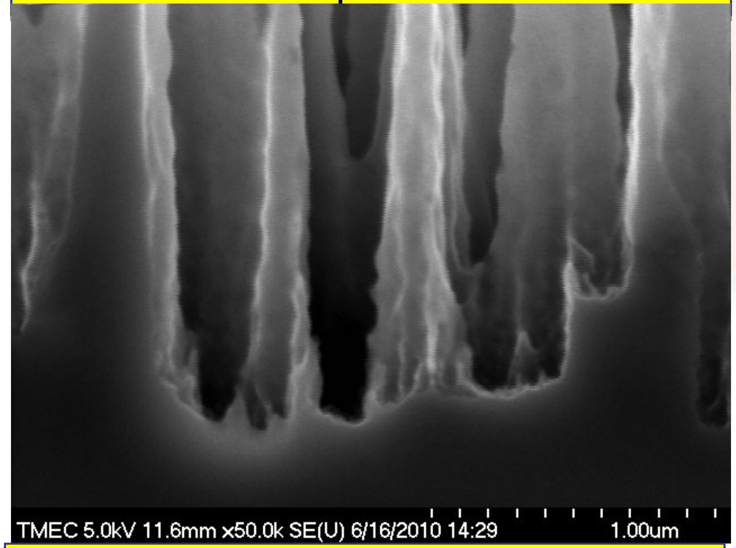


Top view

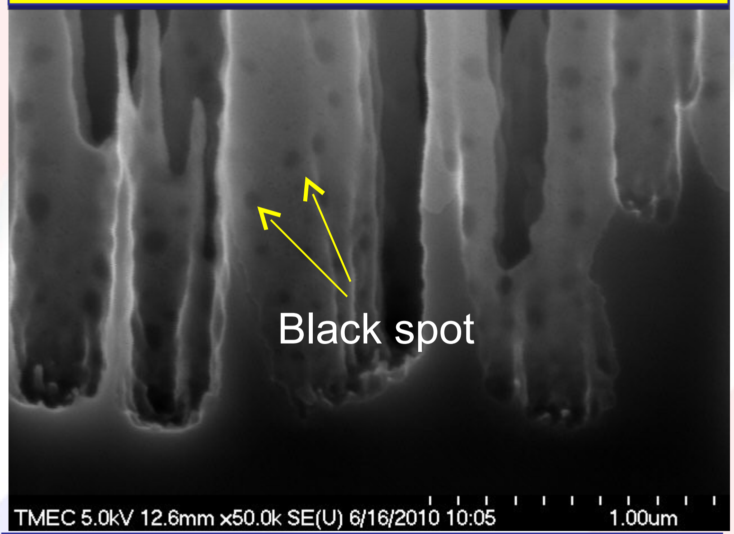


45 degrees side view

Pillar size=250nm
Pillar height=6.5 μm



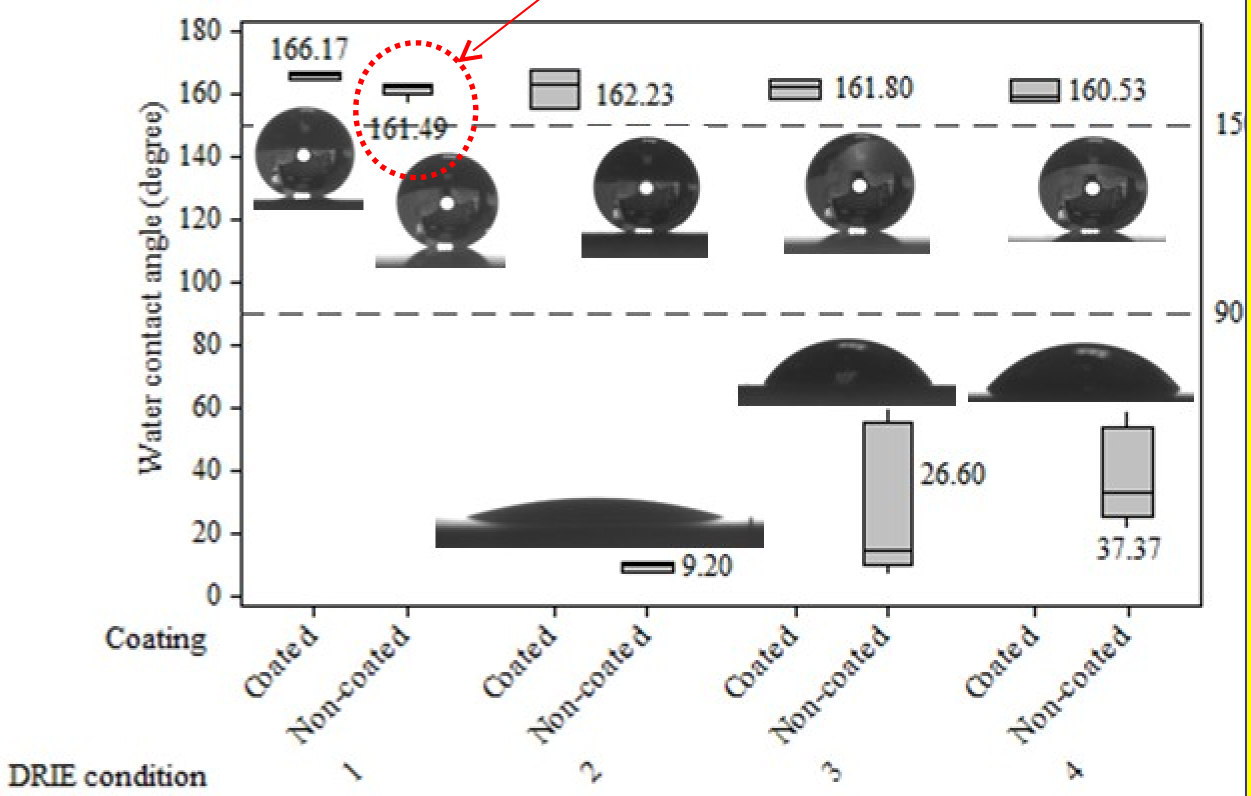
X-view before TPFS coating



X-view after TPFS coating

Water contact angle

Superhydrophobicity without any TPFS coating!!

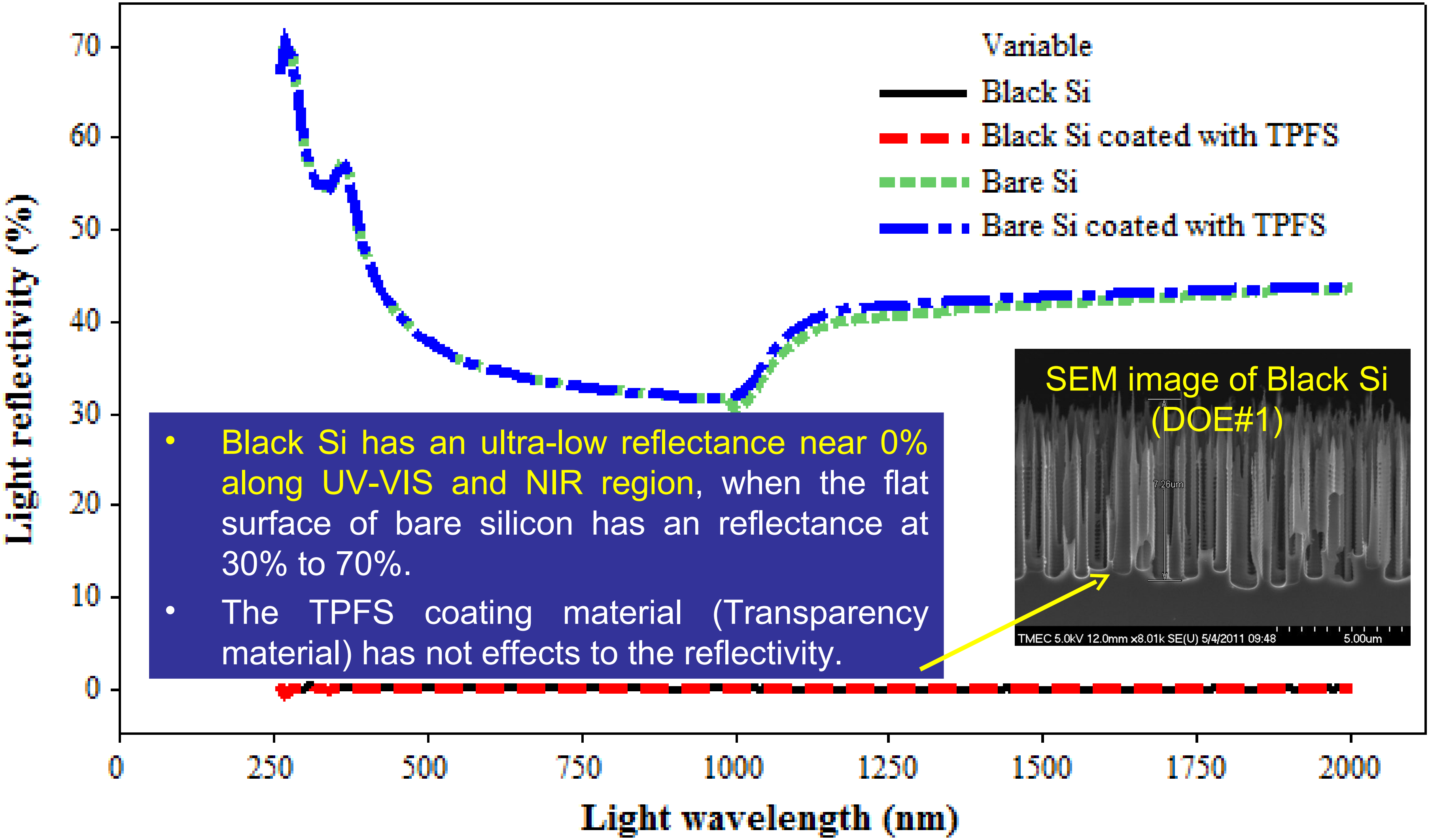


The box plot shown that,

1. The etching condition has an effects to WCA.
1. **The WCA** of the structures made by only Bosch process or only etch **without coated with TPFS is less than 40˚.**
1. The **WCA of RIE+Bosch** process (Deep black silicon) **without coated** with TPFS can make superhydrophobic surface with **WCA = 161.49˚** (DOE#1).
1. **After coated** with TPFS, the **WCA** has increases **above 160˚ for all samples.**

	a (nm)	h (um)	A.R.	Fluorine
DOE1	250	7.0	28.0	Yes
DOE2	250	3.6	14.4	No
DOE3	250	4.1	16.3	Yes
DOE4	113	1.2	0.5	No

Reflectance (Specula @ 8˚)



- Black Si has an ultra-low reflectance near 0% along UV-VIS and NIR region, when the flat surface of bare silicon has an reflectance at 30% to 70%.
- The TPFS coating material (Transparency material) has not effects to the reflectivity.

Reflectance (Specula @ 8˚)

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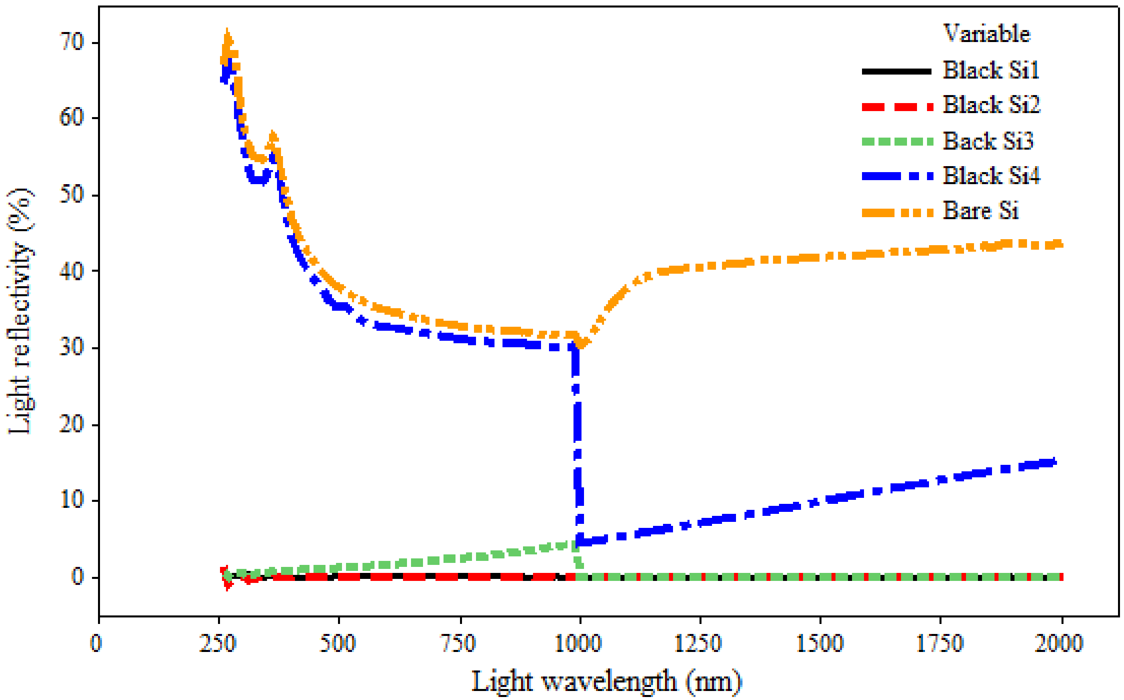
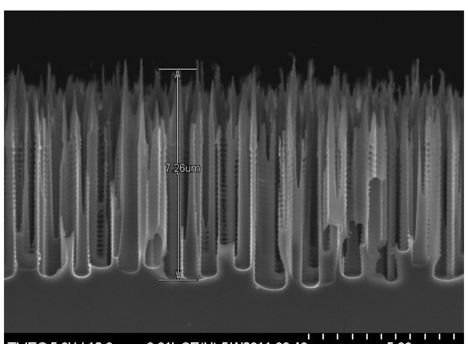
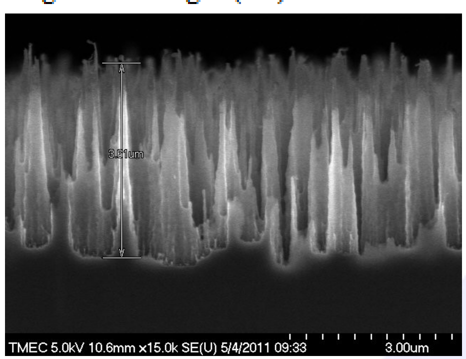


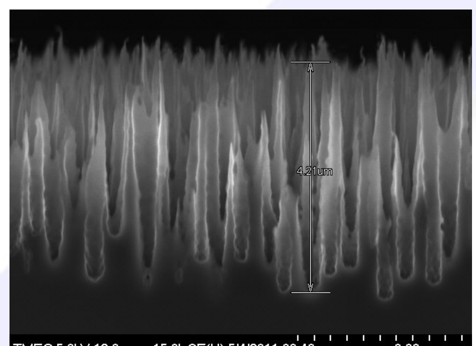
- Difference etching condition make a difference pillar shape and size.
- Pillar shape (depth, size) and its density has an effects to the light reflectivity.



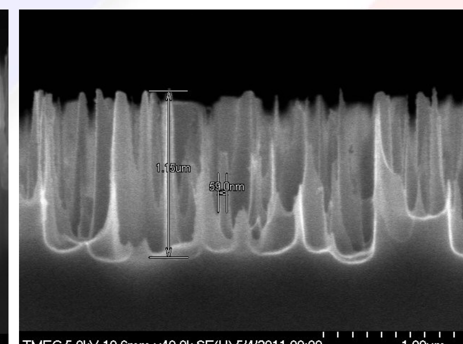
DOE#1
Depth: 7.26 um



DOE#2
Depth: 3.61 um



DOE#3
Depth: 4.21 um



DOE#4
Depth: 1.15 um

Conclusions

1. Black Si can be fabricated by changing an etching condition of fluorine-based DRIE plasma ($SF_6/O_2/CF_4$) especially the **RIE+Bosch process with high O_2 flow rate**.

2. By RIE+Bosch etching, the black Si pillar has attached with black spot, which **AES spectrum shown that its component is Si, C, O , and F**.

3. The black Si pillar size is varied from 113 to 225 nm and the pillar height is varied from 1 to 7 µm. **The pillar size has an effects to WCA and %R**.

4. The **black Si pillar with high A.R.** (a = 250nm, h = 7.0µm, A.R.=28) with F*radical can make a **WCA at 161.49˚** without any coated with TPFS with the **reflectance near 0% at λ = 250-2000nm**.

5. After Black Si was **coated with TPFS**, the WCA has increases to **160˚** and **TPFS has not an effects to the reflectance**.

6. The Black Si can be apply for photodetector, X-ray detector, Night vision camera, etc.

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Deep Reactive Ion Etching (DRIE)

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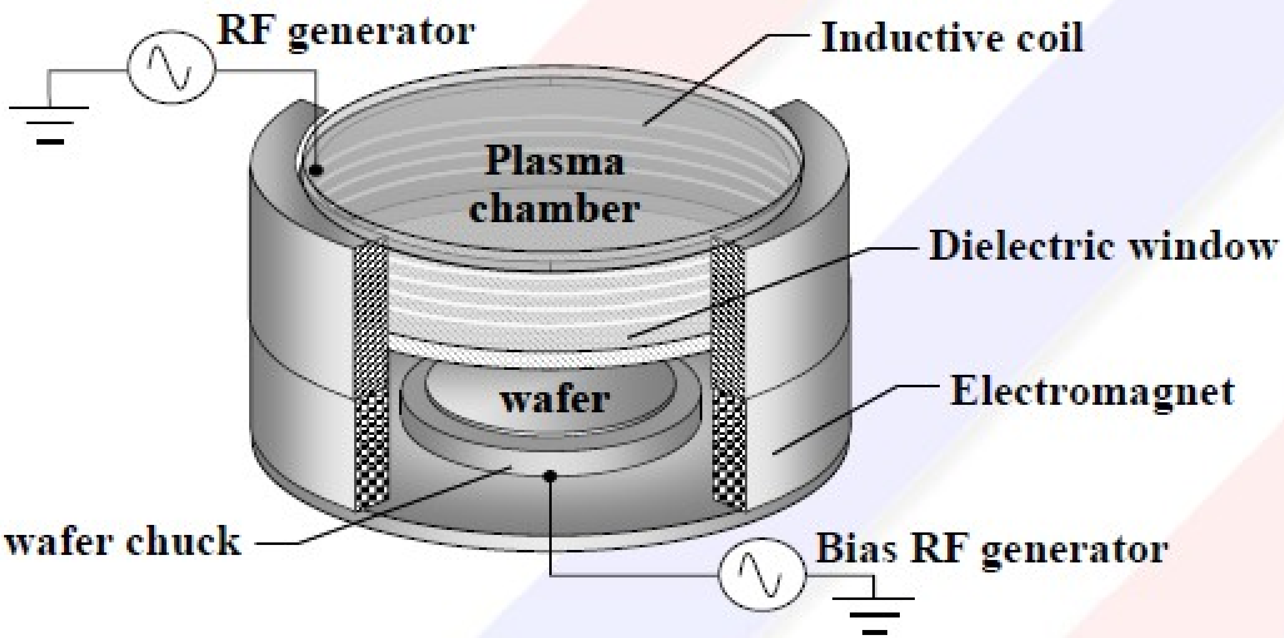
Deep Reactive-Ion Etching (DRIE) is a highly anisotropic etch process used to create deep, steep-sided holes and trenches in wafers.

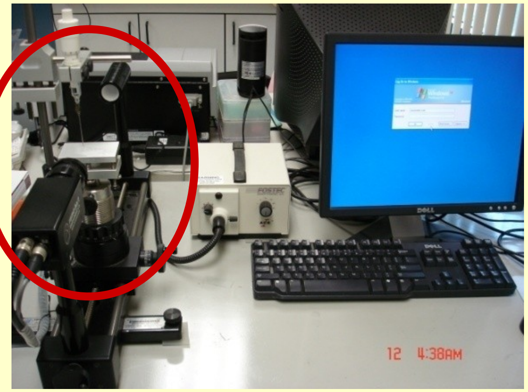
There are two main technologies for high-rate DRIE: cryogenic and Bosch. Both Bosch and cryo processes can fabricate 90° (truly vertical) walls, but often the walls are slightly tapered.



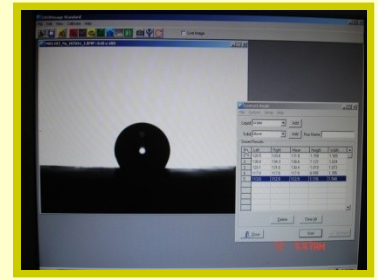
Redrawn from Y. Lii, "Etching," *ULSI Technology*, ed. By C. Chang and S. Sze (New York: McGraw-Hill, 1996), p. 351.

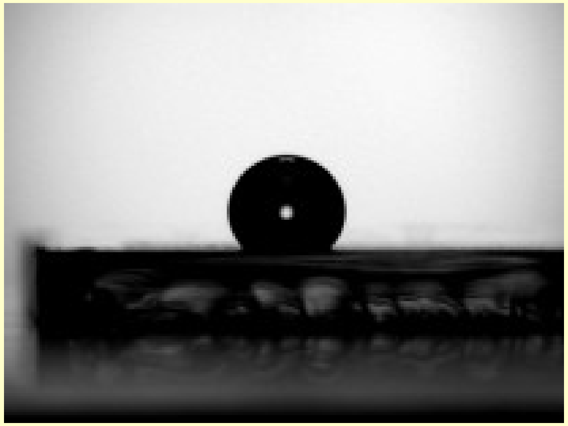
WCA measurement

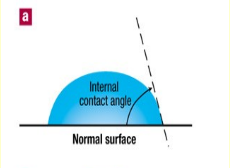
(ramé-hart instrument co.)



Analysis software

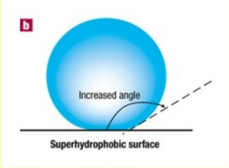






Hydrophilic

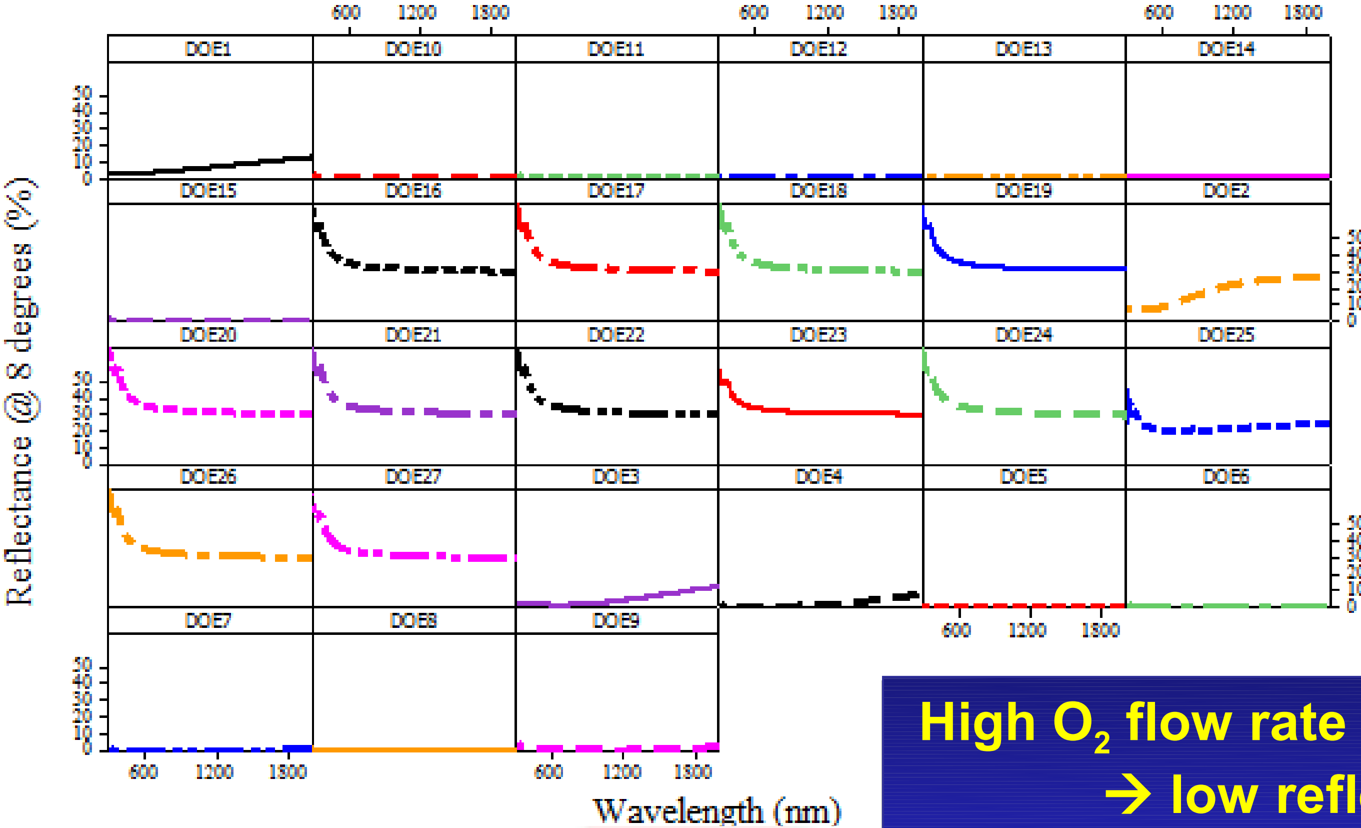
90 ° > θ ≥ 0°



Hydrophobic

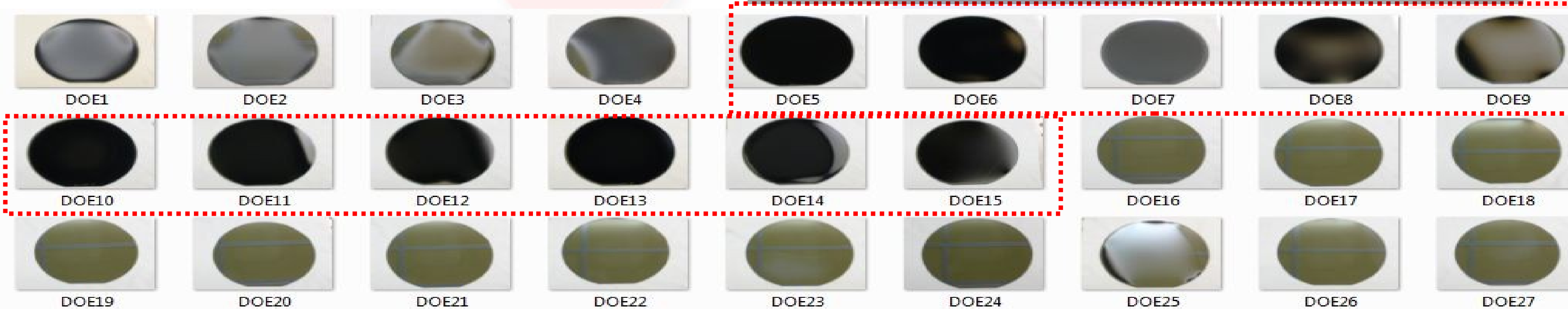
θ ≥ 90°

Ex.2 Reflectance (Specula@8˚)



DOE5-DOE15 has a good reflectance (<10%) in the wavelength of 400-2000nm

High O_2 flow rate → Black surface → low reflectance!!



Ex.2 Effect of A.R. and P after coated with TPFS

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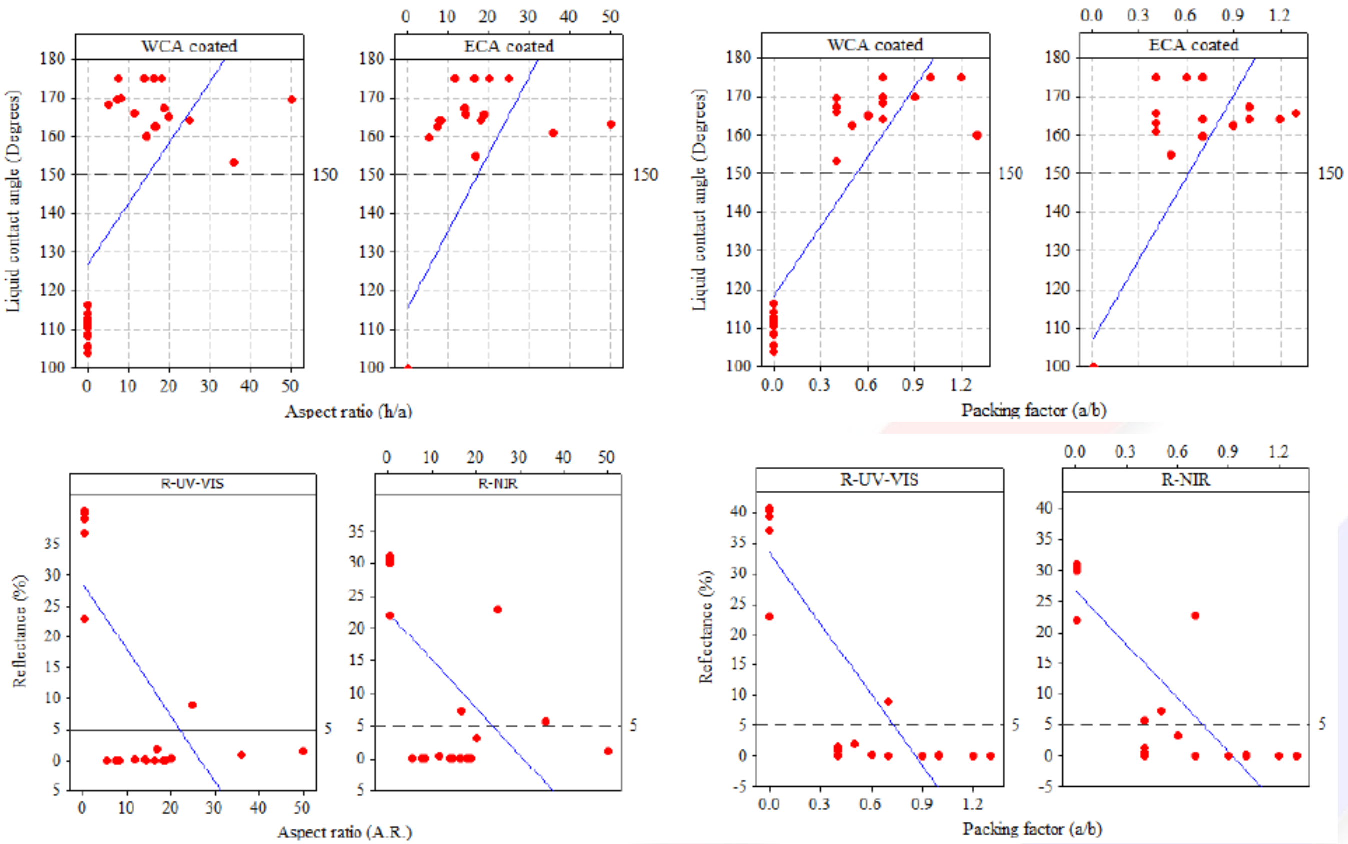

DOE#5: pillar size=396nm, pillar space=576 nm, and pillar height=6.47 µm

Packing factor=0.7 and A.R=16.3

WCA= 175° , ECA= 175°, R(UV-Vis)= 0%, R(NIR)= 0%

The box plot shown that

1. The pillar size has an effects to WCA, ECA and the reflectance.

1. When P and A.R increases, the CA also increases and the reflectance decreases.

1. Smaller and higher black silicon pillar can make a higher WCA and ECA, and a lower reflectance.

2. The best condition is a DOE#5.

Ex.3 Reflectance for Bosch process (Specula@8°)

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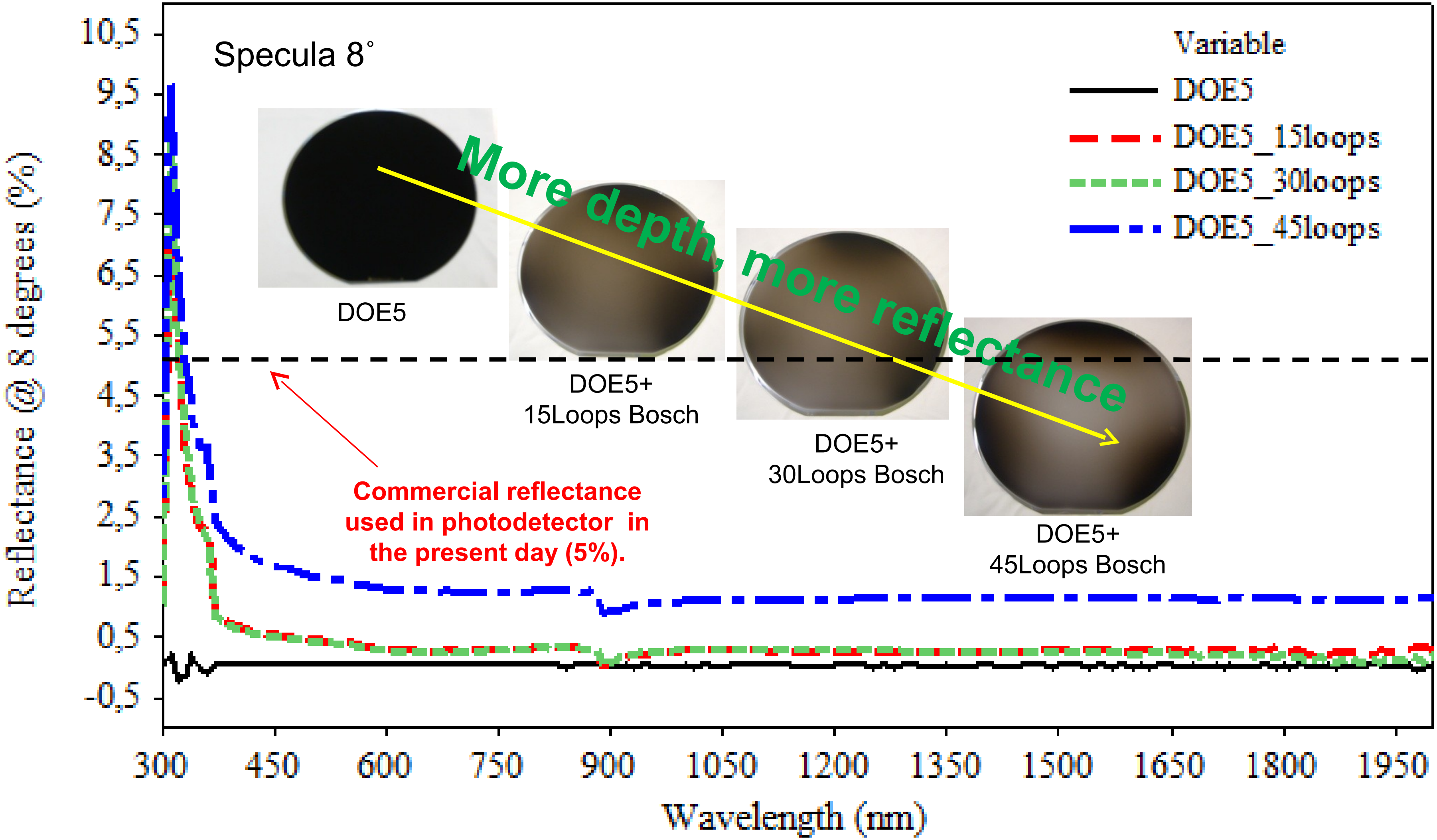

Black Silicon nano-structures