Design and Control of an Anti-Resonance Hybrid Delta-Connected Capacitor Bank for Low-Voltage Industrial Power Systems

Pichai Jintakosonwit

(Sirindhorn International Institute of Technology, Thammasat University)

Sunt Srianthumrong

(National Electronics and Computer Technology Center, NECTEC)

Pichit Jintakosonwit

(Metropolitan Electricity Authority, MEA)

Capacitor Banks for Power Factor Correction

Advantages

- simple structure (Y and △ connections)
- ease of installation
- low cost (compared with SVC or active filter)

Disadvantages

harmonic resonance

between line inductance and capacitance of capacitor banks

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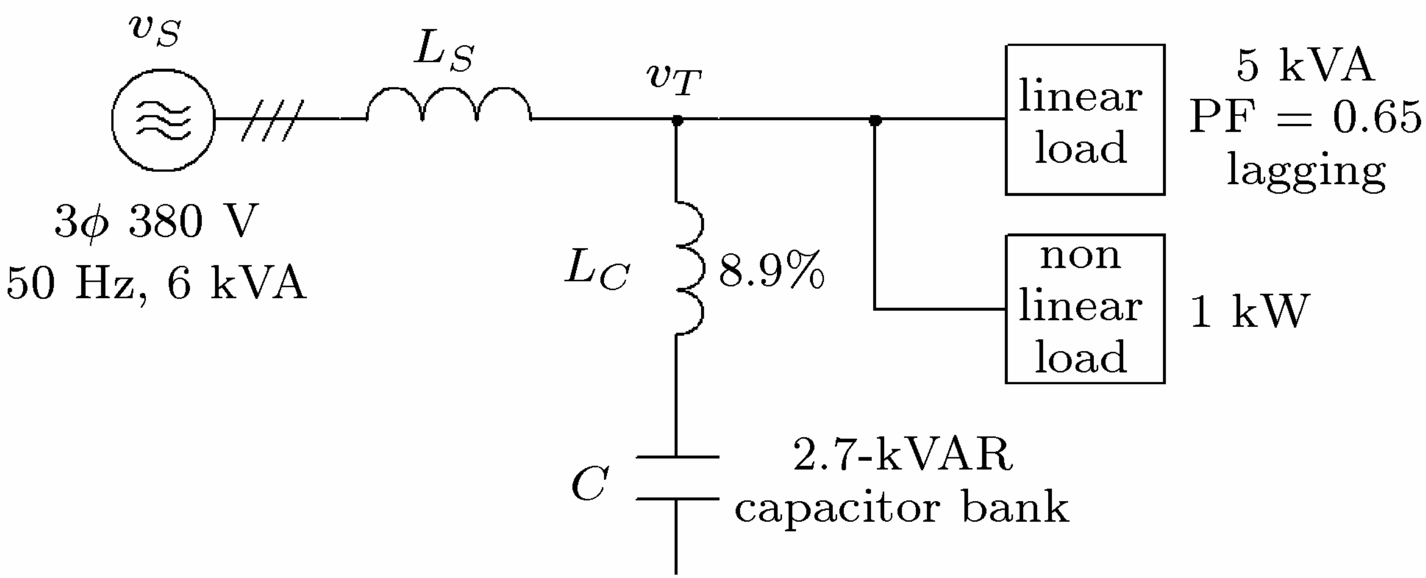
significant amplification of voltage and current harmonics

Capacitor Banks with Resonance Protection



Series capacitor/reactor combination (tuned *LC* filter)

- capacitor C is used to improve the power factor above 0.95.
- tuned frequency is set to the most dominant harmonic frequency.
  (typically the 5th-harmonic frequency)

Research Objectives and Proposed System

In real power systems

uncertain system parameters due to system configurations and loads

→ existence of harmonic resonance even if series capacitor/reactor combination is installed

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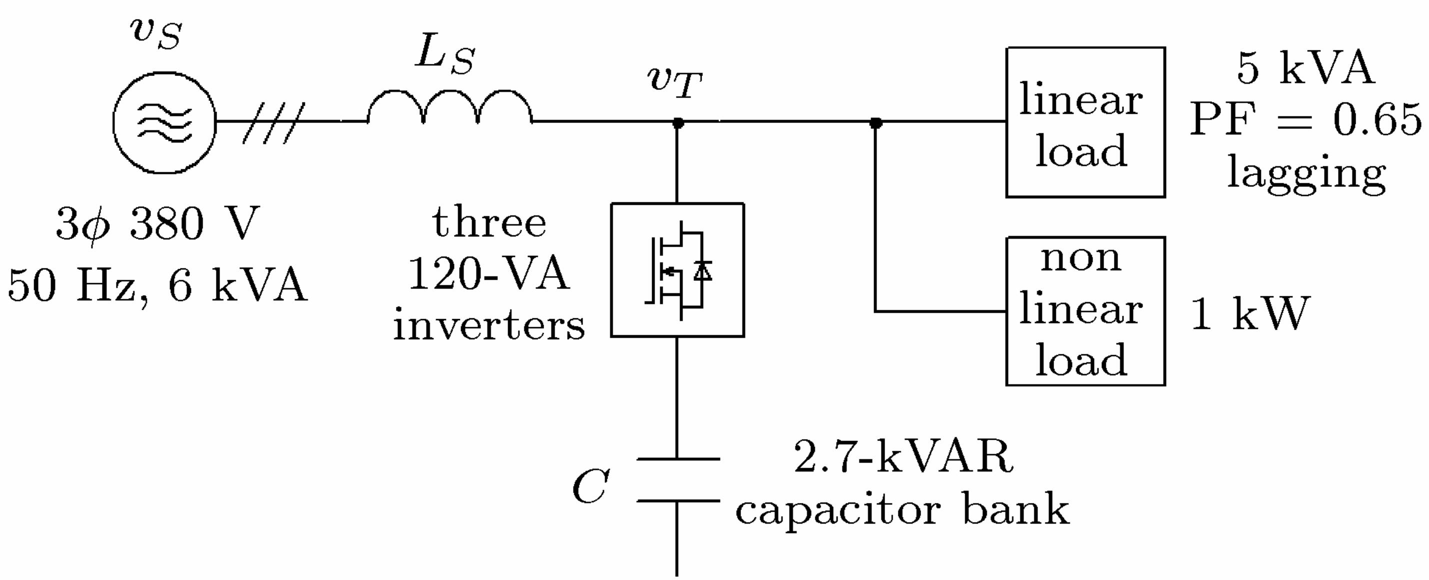
Anti-Resonance Hybrid Delta-Connected Capacitor Bank

Objectives :

compensating for reactive power without harmonic resonance in low-voltage industrial power systems

Hybrid Delta-Connected Capacitor Bank



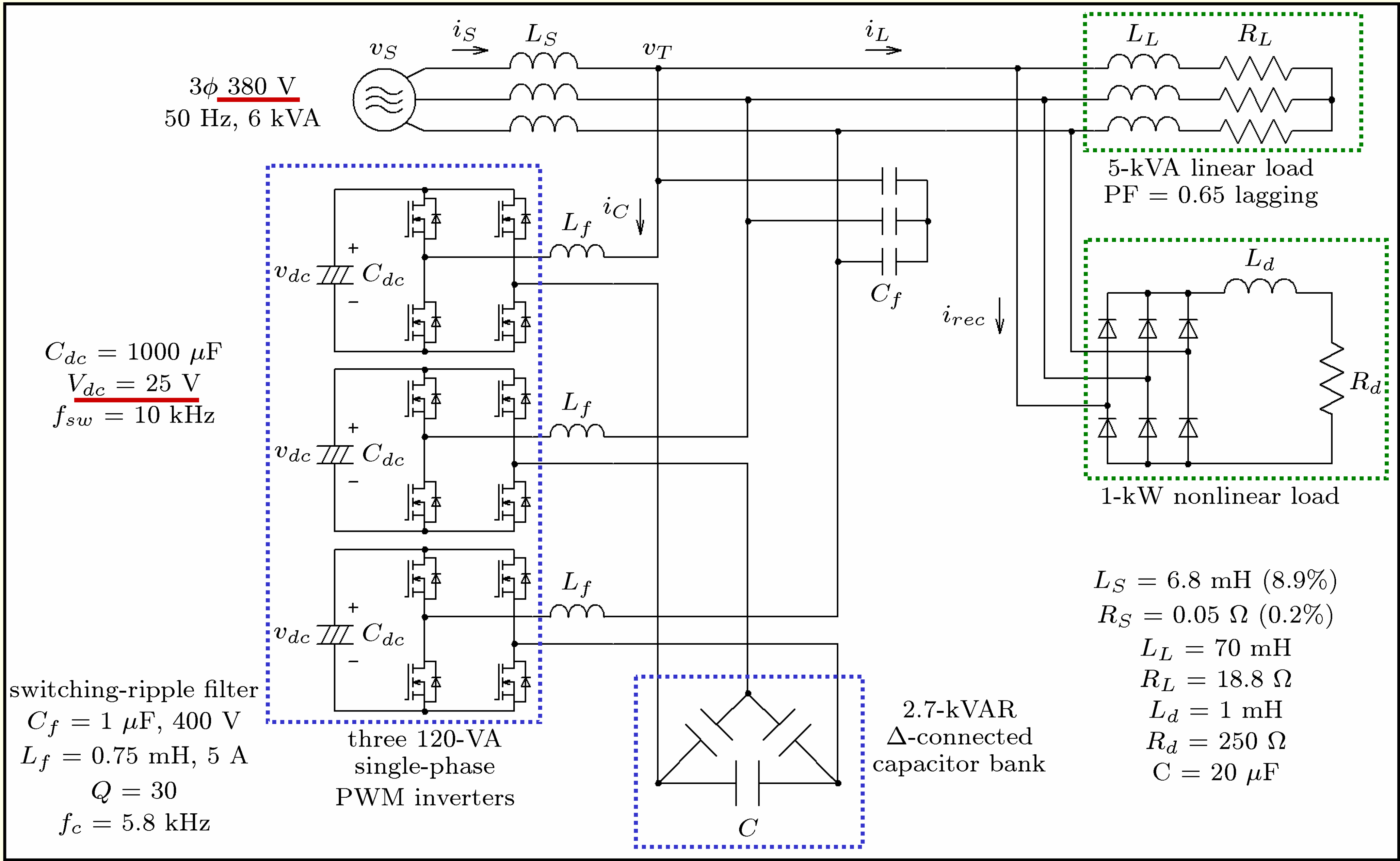
Aim of Capacitor: To compensate for reactive power

Aim of Inverter: To improve characteristic of capacitor

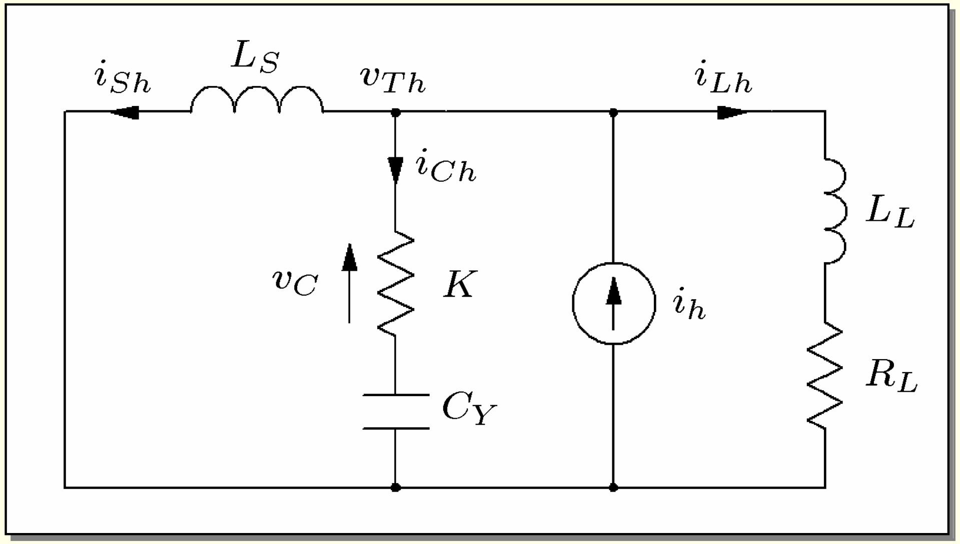
Advantages : low cost, low switching losses,
no resonance, no matching transformer

Drawbacks : complex control, series protection circuit

System Configuration



Principle Operation of Hybrid Capacitor Bank



equivalent circuit

(Note: $C_Y = 3C = 60$ μF)

Control of Inverter

$$v_C = K \cdot i_{Ch}$$

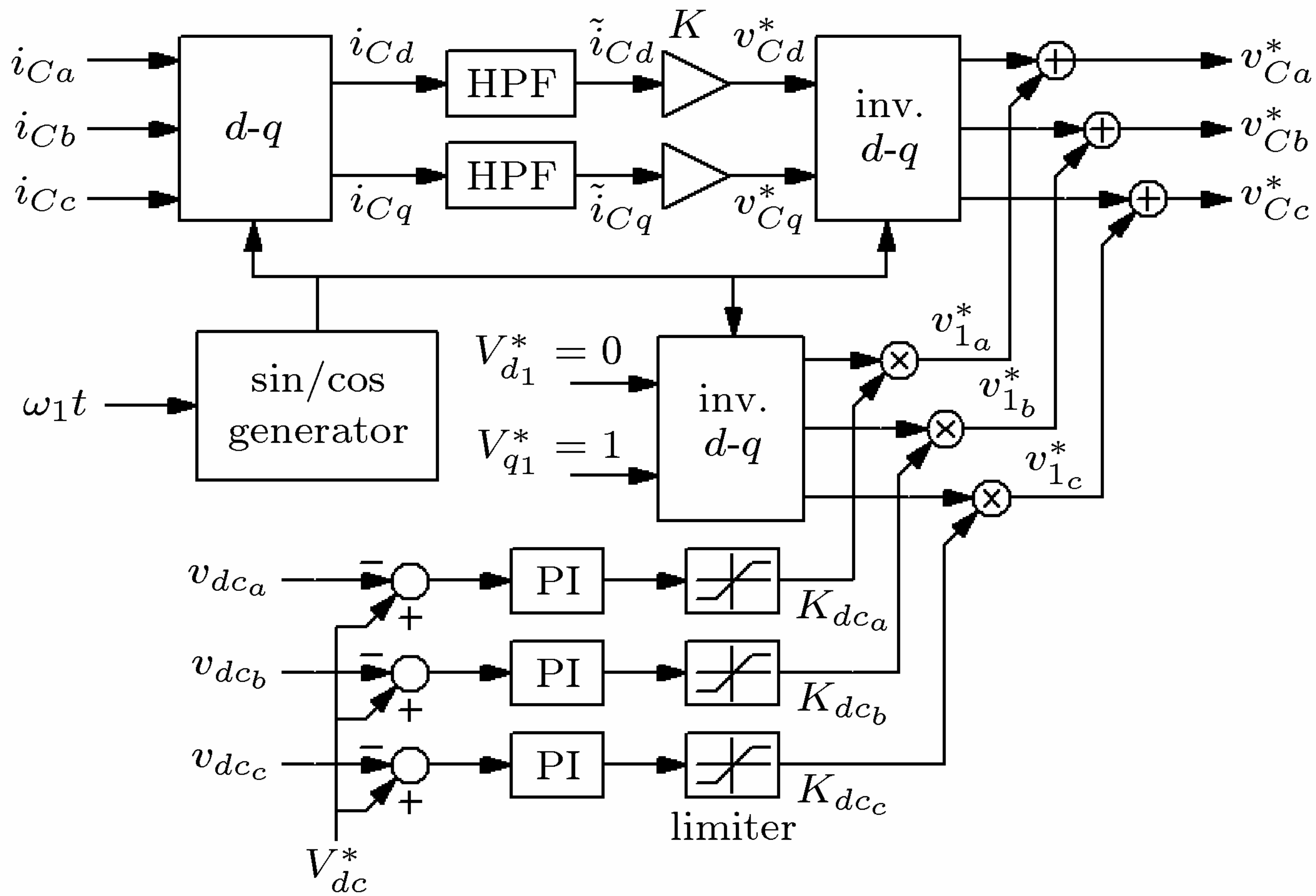
v_C = an inverter voltage [V]

K = a control gain [Ω]

i_{Ch} = a harmonic current in i_C [A]

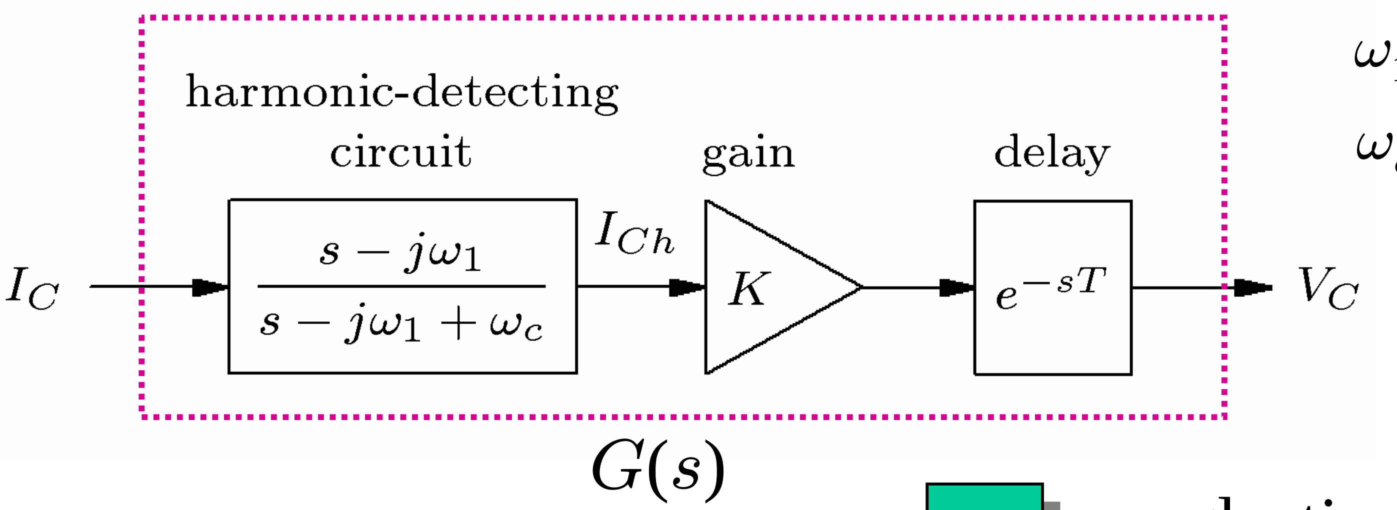
- A zero impedance for the fundamental frequency
- An infinite impedance for dominant harmonic frequencies

Harmonic Detection and DC Voltage Control



- **the PQ theory for harmonic detection**
- **the PI control for dc voltage regulation without any external dc power supply**

Control Block Diagram of Inverter



ω_1 = fundamental frequency

ω_c = cutoff frequency (13 Hz)

time delay T = 50 µs

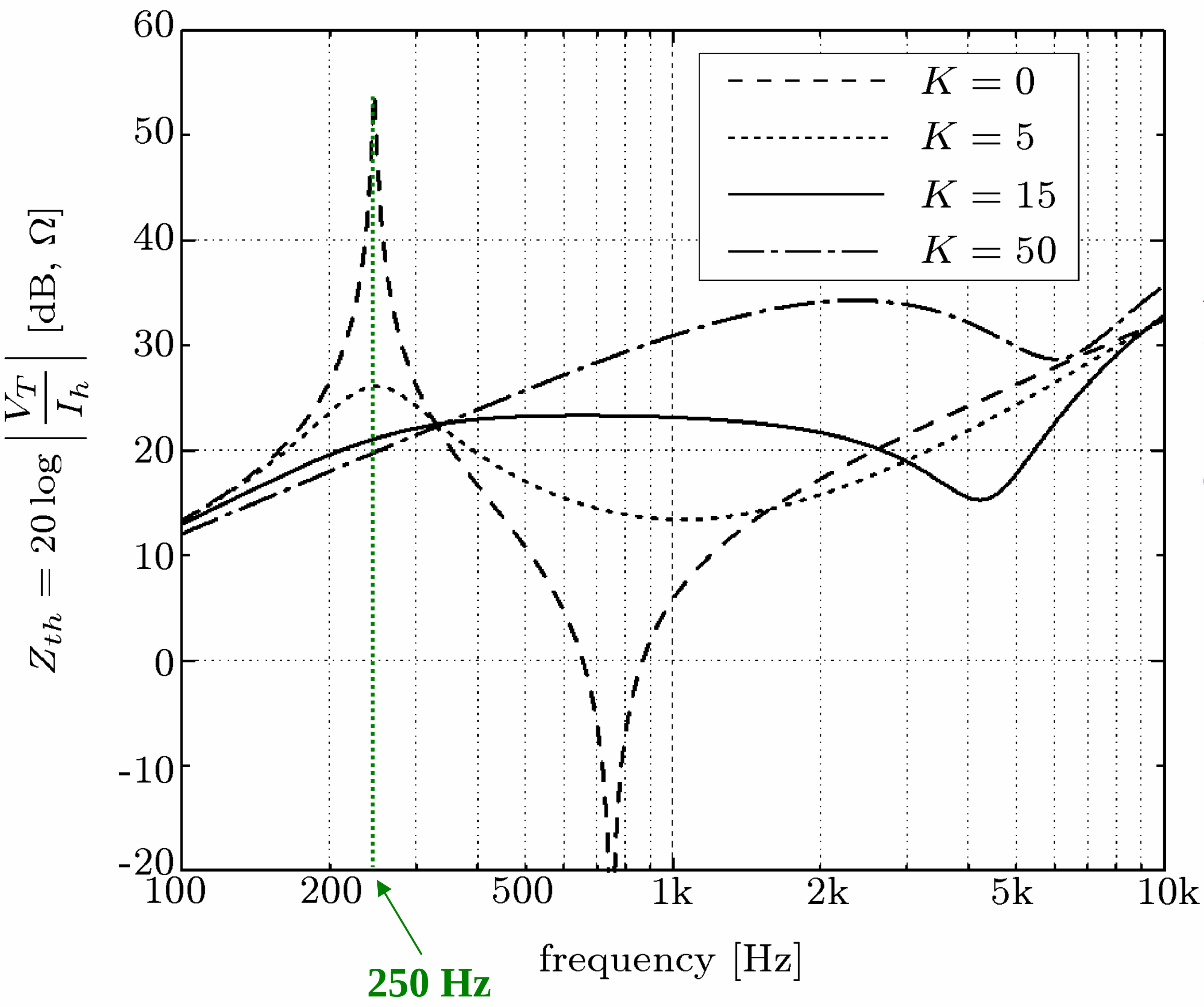
neglecting the effect of ripple capacitor C_f

the impedance looking into the PCC

$$Z_{th} = \frac{V_T}{I_h} = \frac{Z_C + G(s)}{A(s)}$$

where $A(s) = 1 + \frac{Z_C}{Z_S} + \frac{G(s)}{Z_S} + \frac{Z_C}{Z_L} + \frac{G(s)}{Z_L}$

Control Gain Selection



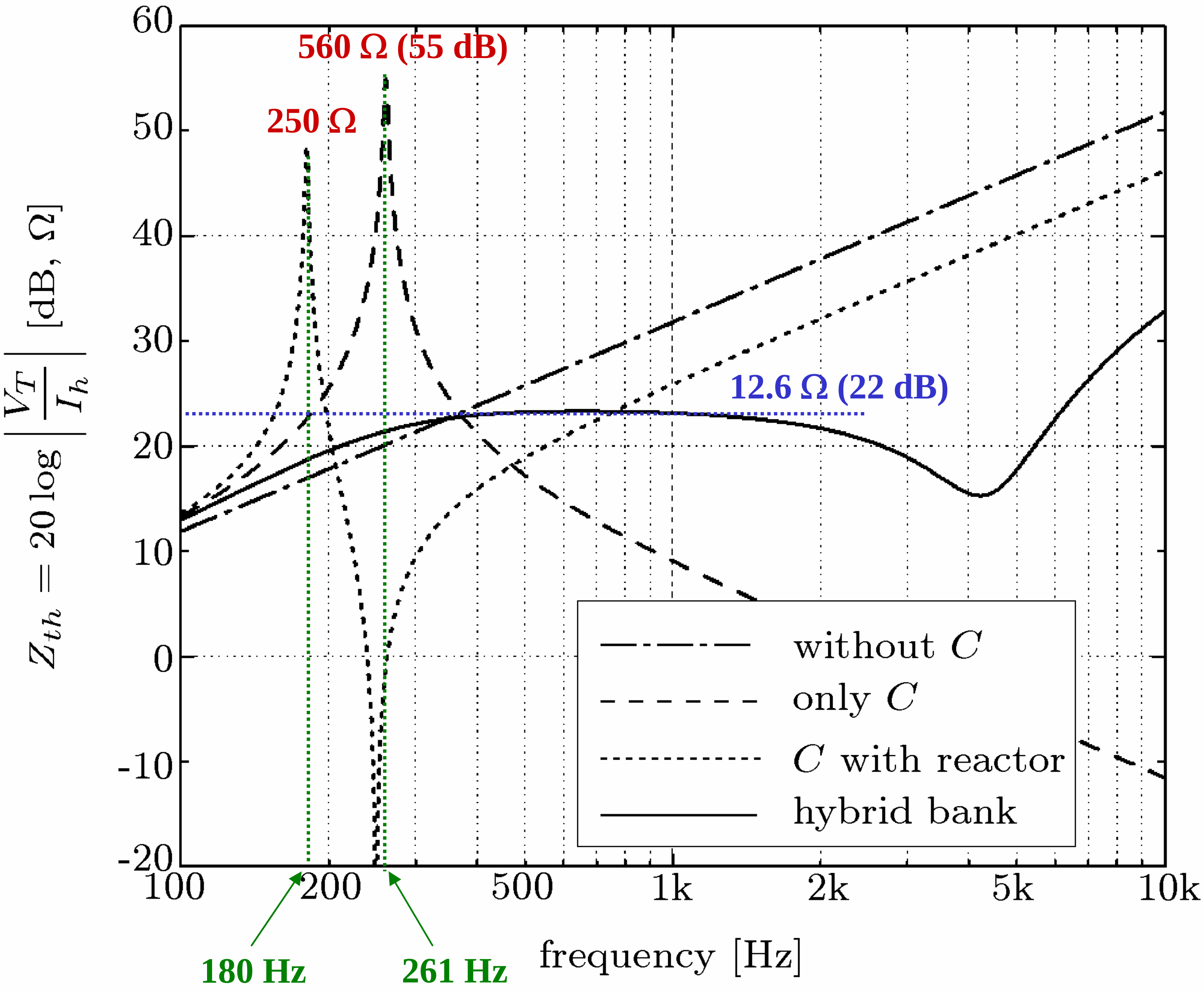
high impedance

high harmonic voltage

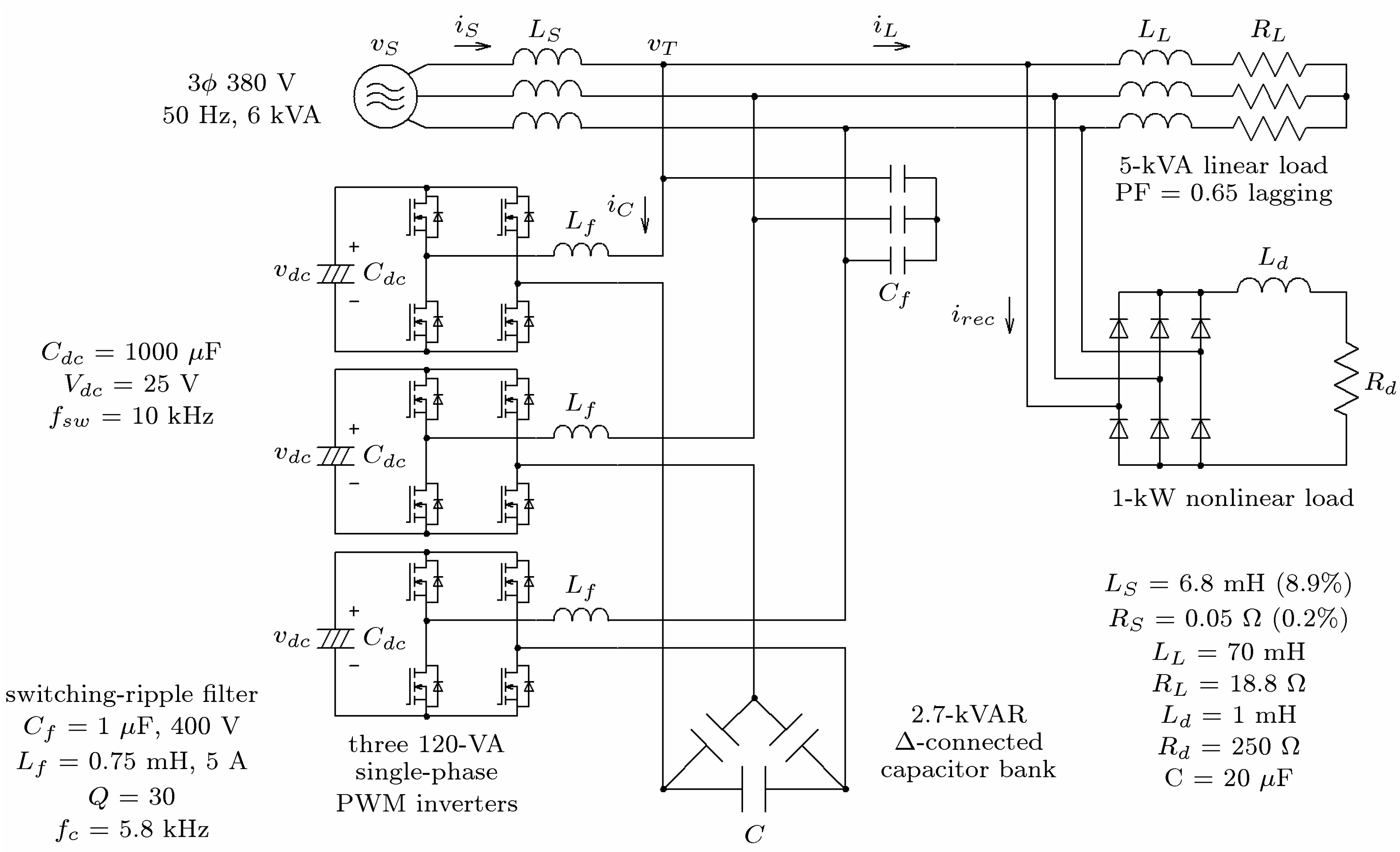
suitable gain

$K = 15\ \Omega$

Harmonic Resonance and Damping

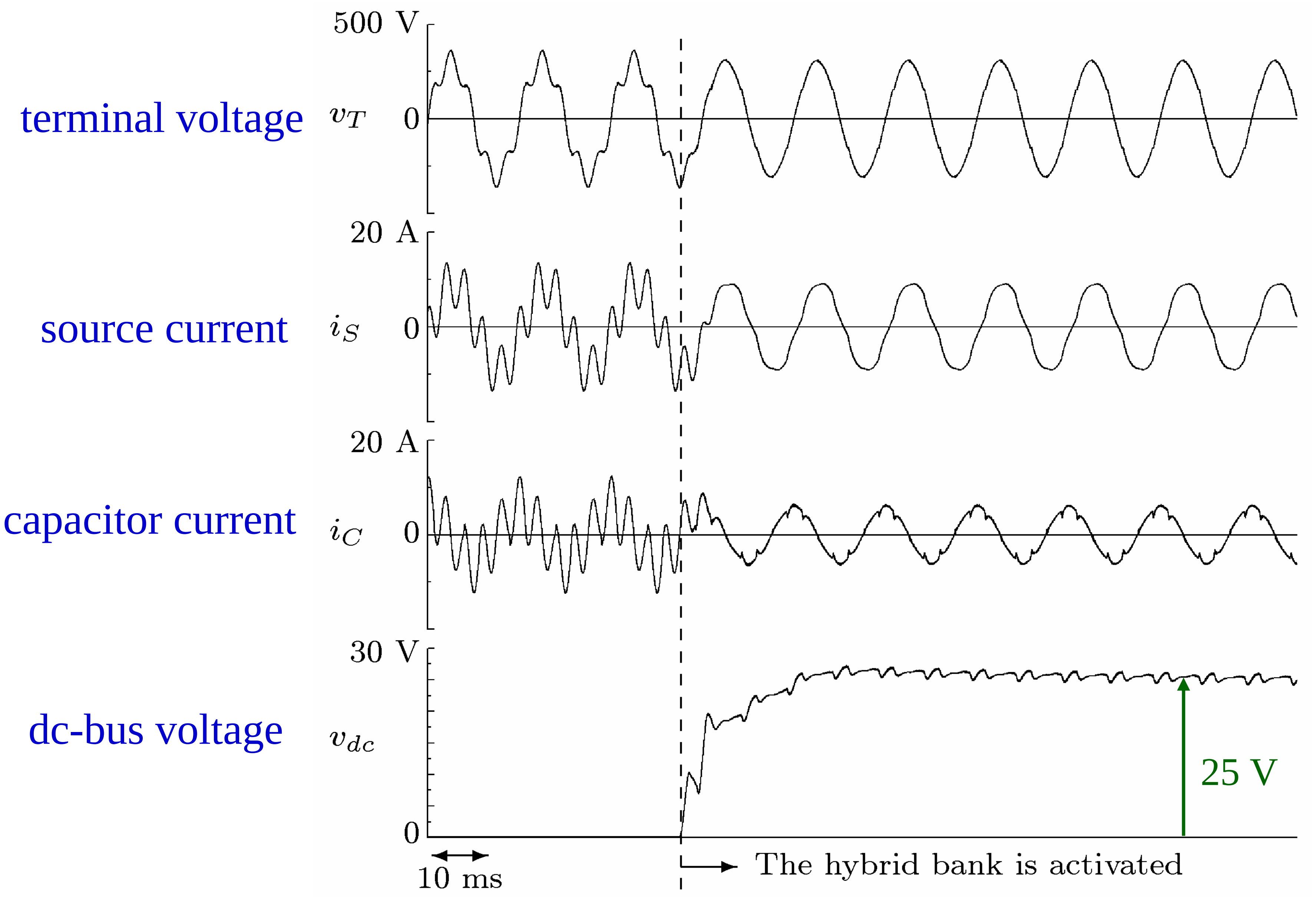


Simulation System under load conditions

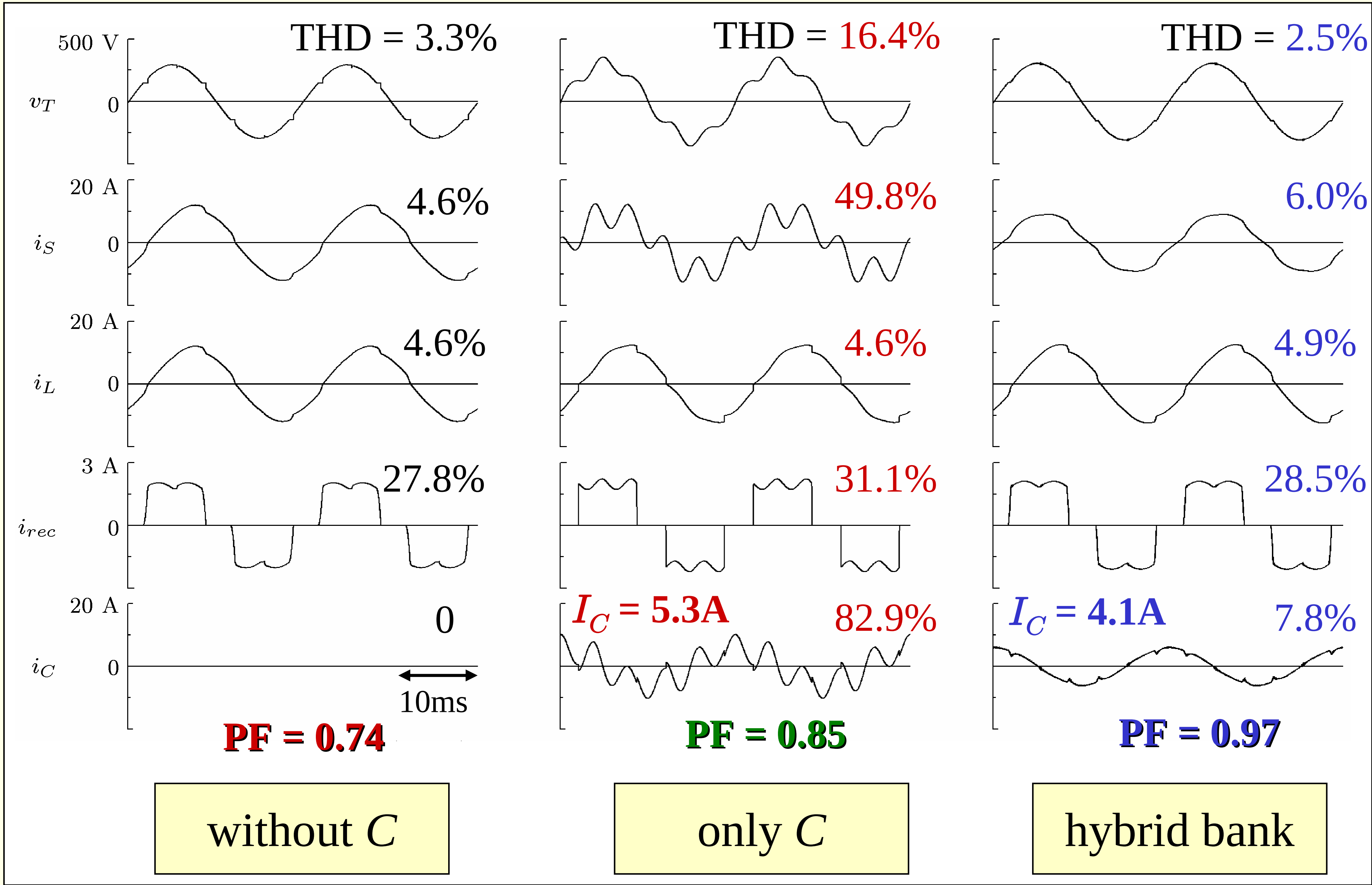


- **The control gain:** $K = 15\ \Omega$
- **The PI gain for dc voltage control:** $K_p = 0.5$ and $K_i = 20\ s^{-1}$

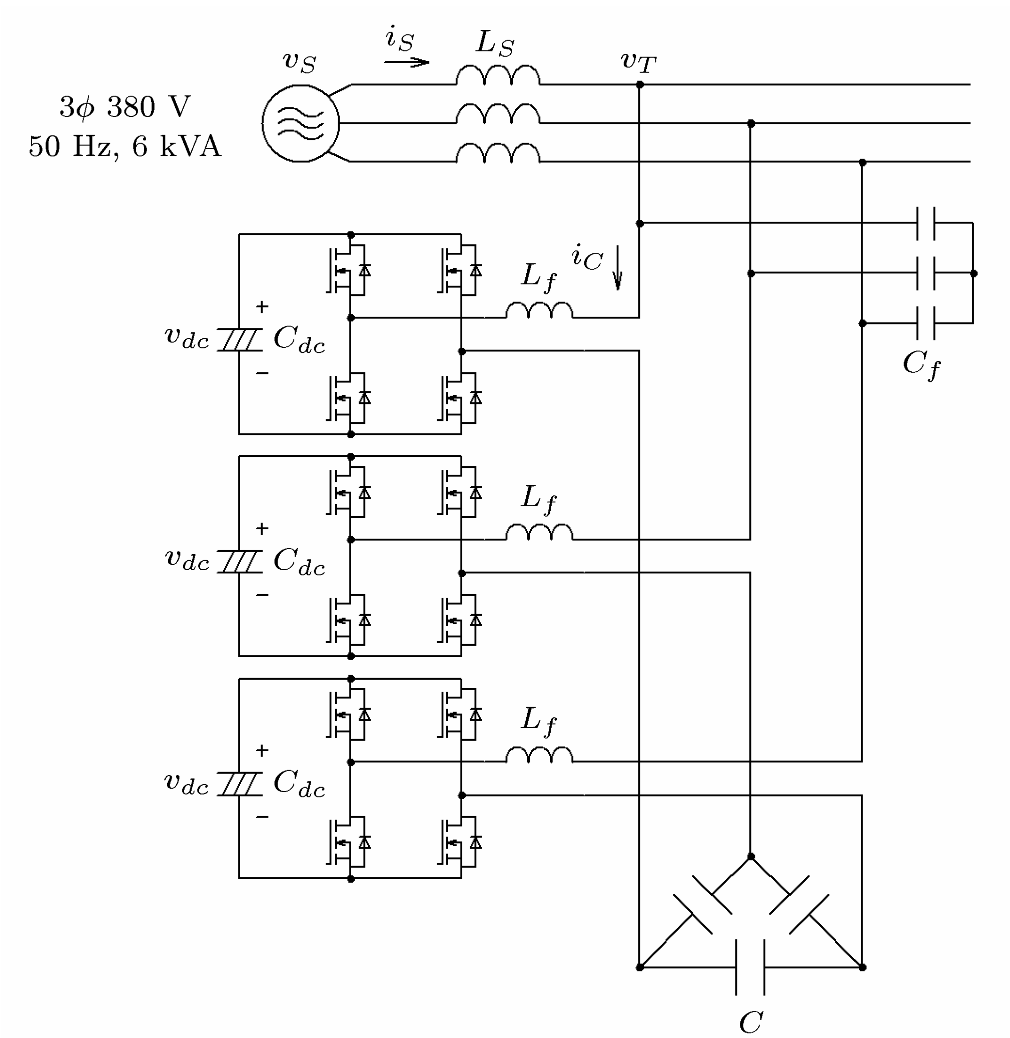
Transient Response



Simulation Results



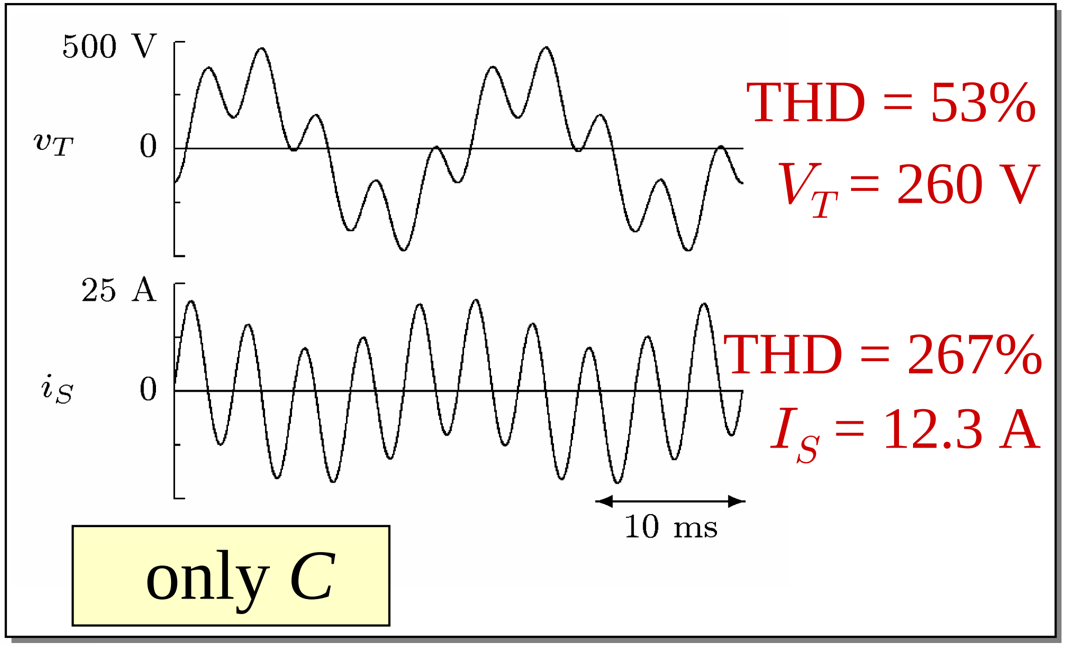
Simulation System under no-load conditions

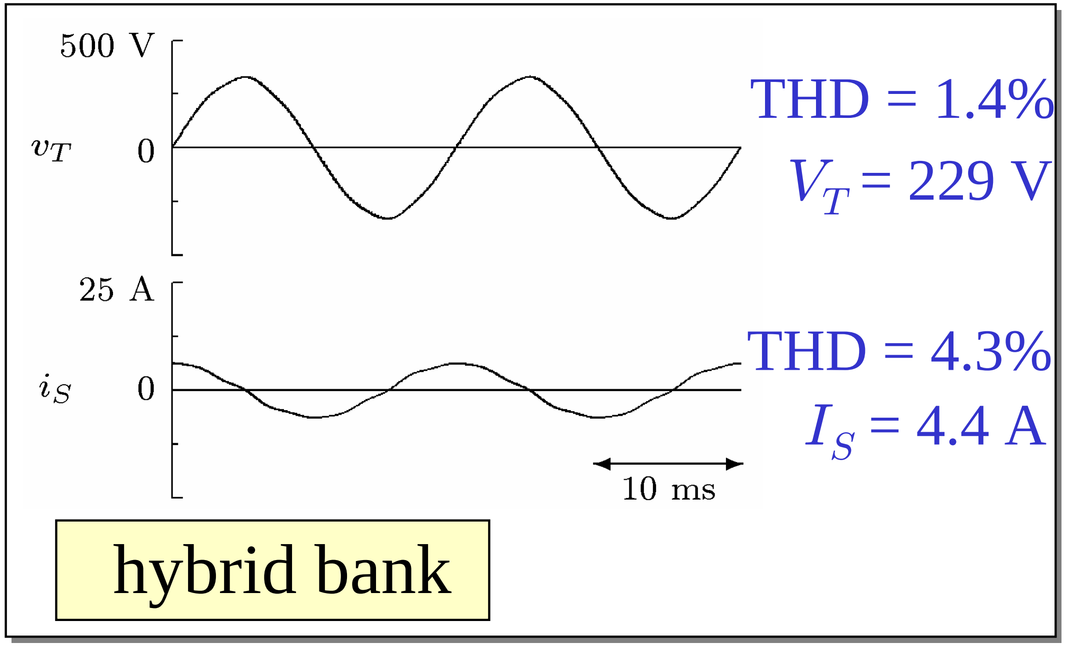


source harmonic voltages

5th harmonic voltage : 1%

7th harmonic voltage : 1%





Conclusion

Anti-Resonance Hybrid Delta-Connected Capacitor Bank

- **△-connected capacitors in series with three single-phase inverters**
- **No matching transformer and external dc supply**
- **Low VA rating, low dc bus voltage and low switching losses**

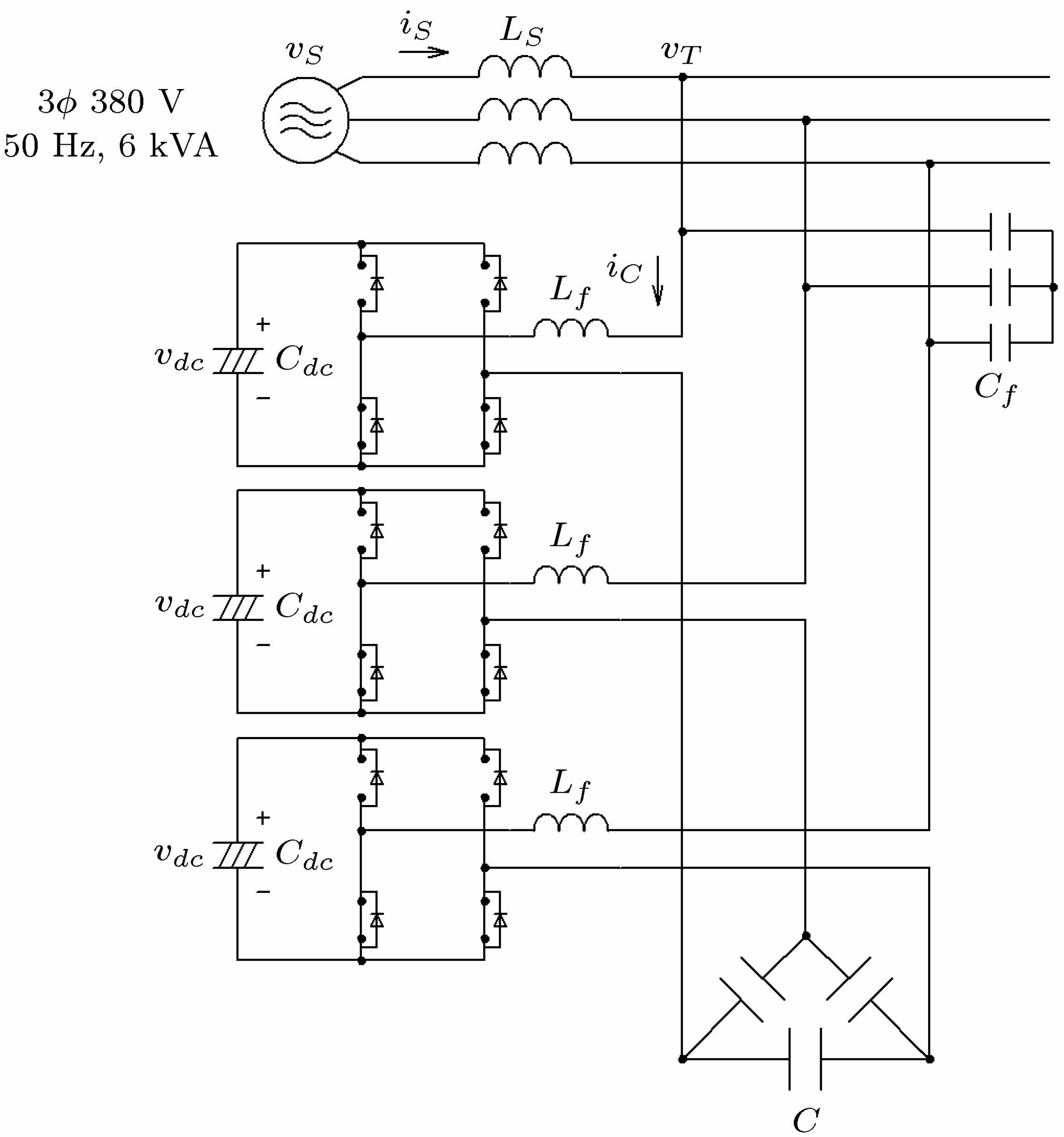
effectiveness of reactive power compensation without harmonic resonance, irrespective of system conditions

Advanced capacitors:

replacing the reactors with the small-rating inverters

existing △-connected capacitors ➡ anti-resonance hybrid capacitors

Protection System



During standby condition:

two lower-arm MOSFETs in each inverter are turned on.

To prevent overvoltage across dc capacitor

Reactive Power Compensation

1. Shunt Capacitor Bank

   Advantages : low cost, simple structure

   Drawbacks : fixed-harmonic compensation, resonance

2. Static Var Compensator (SVC)

   Advantages : unity power factor, no resonance

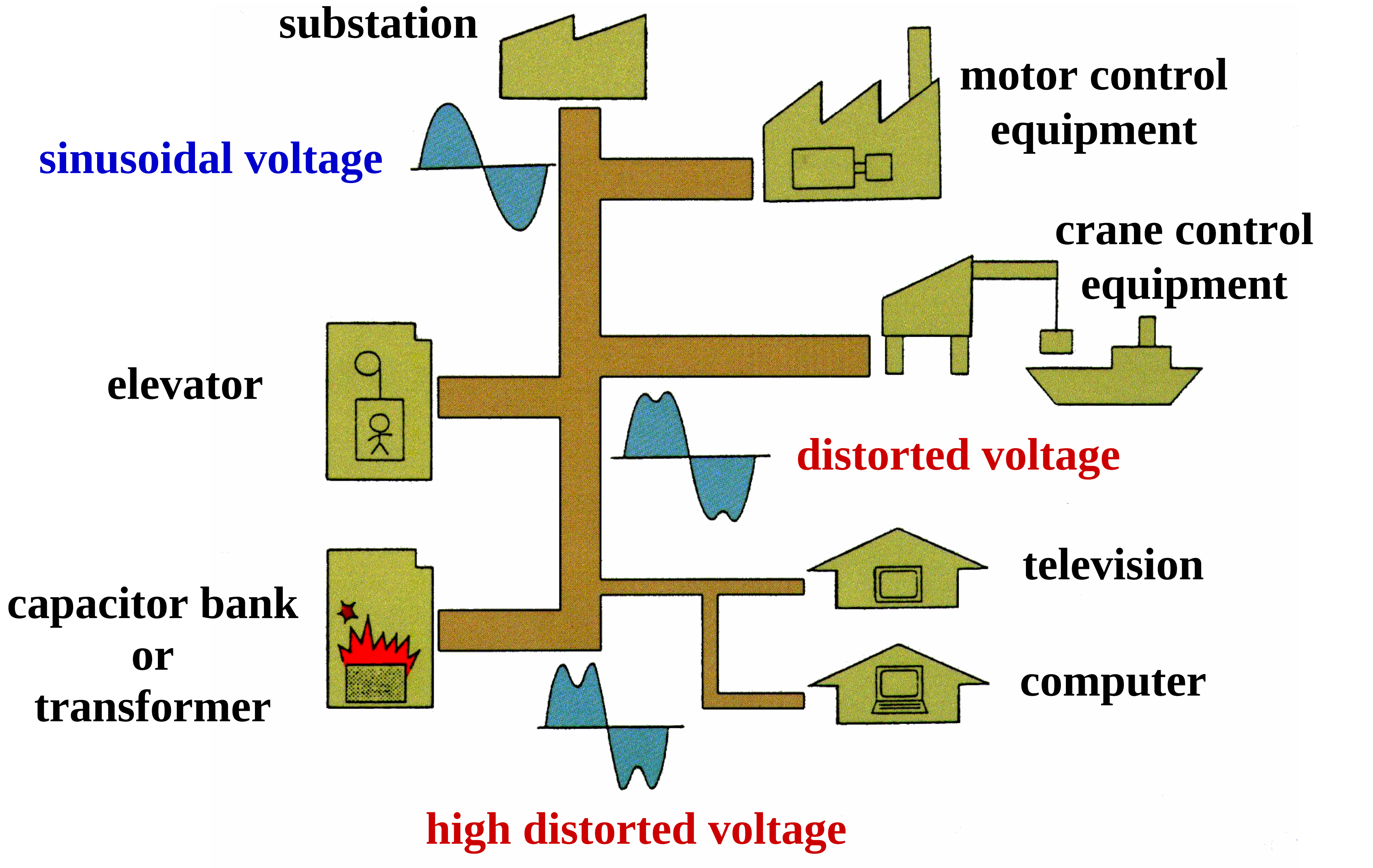
   Drawbacks : high cost, switching losses, complex control

3. Synchronous Condenser

   Advantages : leading or lagging power factor, no resonance

   Drawbacks : starting problem, cooling system

Harmonic Pollution



Inverter Design

IEEE std. 519-1992 : individual harmonic voltage ≤ 3%, THD ≤ 5%

DC voltage

$$V_{inv,LL} = \frac{\sqrt{3}}{2\sqrt{2}} m_a V_d = 3\%$$

Let m_a= 0.8. The required dc voltage is 25 V.

Inverter current

Inverter current = the fundamental current flowing into the capacitor for reactive compensation

The minimum current rating of inverter is 4.2 A.